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Thermal Design: Sounding the Alarm

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Thermal Management Update with Doug Brooks

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I had the opportunity to talk with our regular contributor Doug Brooks recently. He has been doing some research on temperature effects on PCB traces over the last few years, and I wanted to check the status of his latest thermal efforts. He discussed his work with Dr. Johannes Adam, why temperature charts based on a trace in isolation are inaccurate, and how the industry remained so wrong about PCB temperatures.

Andy Shaughnessy: You have done some work on thermal management lately. How did that project start?

Doug Brooks: I wrote an article in the mid-'90s on trace current/temperature effects, and I used two data sources: the then-current IPC data and some data I found in a 1968 Design News (DN) article. The DN temperatures were about 30–40% higher than the IPC temperatures and I wondered why. I began to suspect that it was because of the differences in the way the temperatures were measured or calculated. In looking for a way to confirm that hypothesis, I ran across an article about three years ago written by Dr. Johannes Adam, and I contacted him.


Doug Brooks

It turns out that Johannes had written a computer simulation program called TRM (Thermal Risk Management) [1] that was well suited for me to use to look at the data I had used in the article. He offered me a license for the software and we used TRM to simulate the IPC trace data in IPC-2152 [2] and the earlier data from DN. The simulations were very successful.

Shaughnessy: What did you find out?

Brooks: It turns out the DN data were unreliable!

Shaughnessy: And all of this took place over several years?

Brooks: No. That was just the beginning. It was so easy to simulate the IPC trace data that we began to simulate more realistic scenarios. The IPC data apply to a 6-inch trace in isolation. We began to look at what happens when we change things: change the length, change the pad sizes, add additional adjacent traces, add planes below the trace or on the other side of the board, more common layout conditions like those.

Then we wondered if we could simulate the temperature of a via, something that is difficult to do in practice and to our knowledge had not been done before. When that was successful, we looked at fusing temperatures. This is something I had written about earlier and had developed some basic rules for based on Onderdonk's Equation [3].

That opened some additional insights regarding whether traces heat uniformly or not (they don't). And that opened even more avenues for study. Soon, we had enough new information for a book [4].

Shaughnessy: After all that research, what thermal design issue really stands out in your mind?

Brooks: We discovered several very interesting insights, but by far the most dramatic was how wrong we had all been regarding via temperatures. Our industry-wide rule of thumb has been that a via's cross-sectional area should be the same as the trace cross-sectional area. If it is not, then multiple vias should be used [5]. It turns out that if the cross-sectional areas are equal, then the via is cooler than the trace. And if not, the via can take a lot more current than we had imagined. In most cases, if the trace has been sized correctly, only a single, small via is needed, almost regardless of current level.

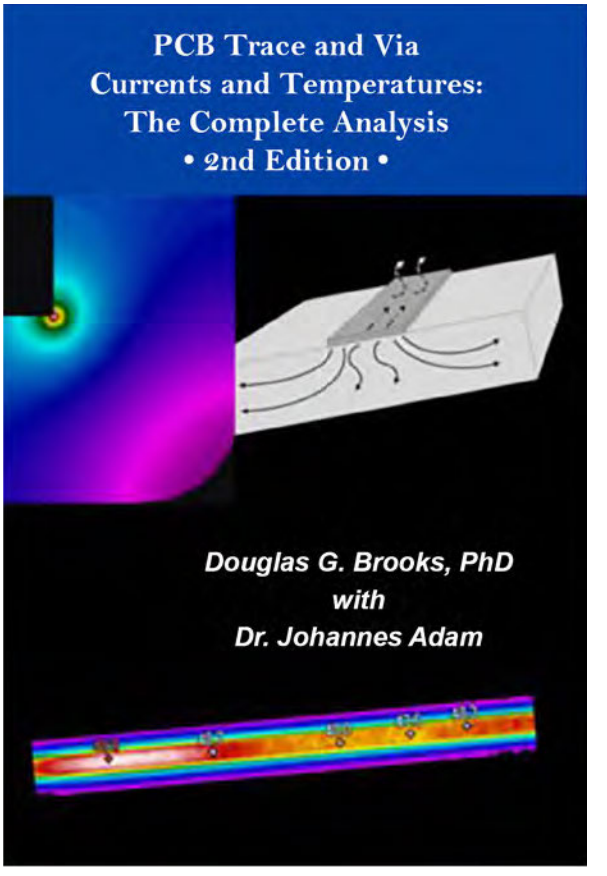

Figure 1: Doug Brooks recently collaborated with Johannes Adam on this book, and their research yielded some interesting results.

Shaughnessy: How can you get by with a single, small via, and regardless of current? That seems counterintuitive.

Brooks: The reason is that the via length is very small compared to the trace. The trace acts as a heat sink for the via and conducts heat away from the via. We can easily push two to three times the expected current (and more) through a via, and the heat-sinking properties of the trace will keep the via temperature under control. These results are explained in detail in Chapter 7 of the book.

Shaughnessy: That result was based on simulations. Is that when the experimental work started?

Brooks: Yes. We knew that no one would accept those results without experimental verification. I went to Prototron Circuits in Redmond, Washington, and asked if they would provide some test boards for us. They were very generous in providing via test boards, and then several other boards for subsequent testing. The via experimental results confirmed the simulations, as described in Chapter 9 of the book. I could not have done everything that I did in the book without Prototron's contribution.

I was extremely fortunate that everyone asked for support was willing to help. Eight persons or companies are mentioned in the "Acknowledgement" section in the book, each of which provided invaluable services or advice. For example, C-Therm Technologies (Fredericton, New Brunswick) took board material samples and measured the thermal conductivity coefficients for us. The Jesse Garant Metrology Center (Windsor, Ontario) took X-rays of the via board for us. I am very grateful for it and humbled by it.

Shaughnessy: After all that, is there any general conclusion regarding trace currents and temperatures that you'd like to share?

Brooks: I'd like to highlight two. First, the IPC-2152 data are worst-case. By that, I mean that a single trace in isolation is a worst case. The data are correct, but we almost never have a trace in isolation. Anything we do in a real-world design sense lowers the temperature.

Second, all this stuff is too complicated to analyze with graphs or equations. Our industry has been here before. In the early '90s, many designers began to worry about and deal with controlled impedance traces. Back then, we used equations published in documents from IPC, Motorola, and National Semiconductor. Today, we now know that those equations are not adequate, and we need field-effect solutions for calculating trace impedance. The same thing is happening for trace current/temperature relationships. If we want to optimize our designs, we need to use thermal simulation tools.

> "If we want to optimize our designs, we need to use thermal simulation tools."

Shaughnessy: What's your next project regarding thermal management?

Brooks: Right after I gave a presentation on this topic in Tel Aviv last May, I was approached by Mentor's Nitin Bhagwath, who was really thinking outside the box. As we talked, we realized that there are two design paradigms board designers need to understand: The first is how to move the signal (current) from point A to point B. As rise times get faster, we have to start dealing with various signal integrity issues. As an industry, we already have a good understanding of how to do this. The second is how to move the power from one place to another. This is quite different from moving a signal. As the current increases, the I^2R drop increases, increasing the trace temperature (heating the trace). We need to manage this heat buildup and dissipate it some way. Currently, our primary answer is to increase the trace size, usually using the data in IPC 2152. But Nitin pointed out that there are other, perhaps many other, tricks we can use to manage the heat dissipation without impacting signal integrity. Many of these tricks employ the addition of non-current carrying areas of copper along the trace to increase the surface area, where we can, and ways to reduce the area in places where there is a high density of interconnects. Nitin will be presenting a paper on this with numerous examples at DesignCon in January. I have co-authored that paper with him, along with five other people [6]. I am excited about this new insight.

Shaughnessy: What's next for Doug Brooks? Didn't you say you were going to retire?

Brooks: I have been threatening retirement for about four years now. The time has finally come. My wife and I have just downsized into a condo near Seattle, and I am spending my time watching sports on a huge TV and playing with our seven grandchildren.

Shaughnessy: And writing articles for us! Thanks for talking with me, Doug.

Brooks: Thank you. **PCBDESIGN**

References

1. TRM (Thermal Risk Management) was originally conceived and designed to analyze temperatures across a circuit board, taking into consideration the complete trace layout with optional Joule heating as well as various components and their own contributions to heat generation. You can learn more about it by clicking here.

2. IPC-2152, "Standard for Determining Current Carrying Capacity in Printed Board Design," August 2009

3. This first article, "Fusing Current: When Traces Melt Without a Trace," was published in Printed Circuit Design, (Miller Freeman), in December 1998. It has been withdrawn from the UltraCAD website because of the new information we have discovered in this research.

4. Douglas G. Brooks and Johannes Adam, *PCB Trace and Via Temperatures: The Complete Analysis, 2nd Edition, 2017,* available at Amazon.com.

5. IPC-2152, op. cit., page 26.

6. The other co-authors are Robin Bornoff, Praveen Anmoula, and Pat Carrier (Mentor Graphics), Joseph Aday (Raytheon), and Robert Carter (Oak-Mitsui).