Thermal Management:
Don't Believe the Datasheets

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We all know that the temperature of components and materials in a PCB must not exceed a limit between 100°C and 150°C. When the environment is already hot or when heat dissipation is impeded, it is important to be aware of this as early as possible so that appropriate action can be considered and initiated. Compliance with the thermal specifications is not everything, but it is one of the necessary steps in electronics development.

Simple Temperature Predictions: Likely Wrong

What are some methods for predicting the temperature of a PCB? You could take the datasheet of the component and search for temperature information (e.g., for the maximum power dissipation P_{max} or the junction-to-ambient thermal resistance $R_{\Theta J\text{-}A}$). Both are in relation to each other via $T_{max} \approx T_A + P_{max} \times R_{\Theta J\text{-}A}$. The formula is simple but, unfortunately, not to be recommended because "ambient" really includes everything around the component,

from the pad to the vias, and the design of the layers up to the air. We can easily imagine that $R_{\Theta J\text{-}A}$ cannot be a "material constant" of the component. On a good thermally conductive copper plate, the same heat source (the component) would have a much lower temperature than on a plate made of FR-4 and thus a different J-A thermal resistance. The PCB on which the datasheet is based plays an important role.

The test environment for the datasheets is usually based on a PCB with a minimalistic design, according to JESD-51 [1]. A review with examples is given by Edwards and Nguyen [2]. Due to the deviation between the real environment and the test environment, $R_{\Theta J\text{-}A}$ must not be used for temperature predictions (Wong [3] p. 4). $R\Theta J\text{-}A$ is used rather as an indicator for comparing the thermal properties of different components, which are tested under comparable environmental conditions. There is another often misused version of thermal resistance, derived from the Fourier differential equation of heat conduction, namely that for a plate according to $R_{th} = \text{thickness} / (\text{area} \times \text{thermal conductivity})$. This simplification is only valid

for a one-dimensional adiabatic heat transport through (e.g., a thin heat conducting sheet), but it cannot describe the heat spreading in the board (not even in a homogeneous plate). Therefore, it is obvious that there is no panacea for temperature prediction.

Simulation: A Better Way to Predict Temps

A numerical analysis can cover both the big picture and the details for better prediction. What makes a PCB a complex geometry is the sequence of copper layers and prepregs, the stackup, the pattern of the copper tracks in the layers, the artwork or layout, and the placement of the components. Let's look at a few examples. These calculations were performed with Thermal Risk Management (TRM) software, which was developed by my company ADAM Research and can be used by the users of all ECAD systems by importing standard files (e.g., Gerber, drill files, netlists, text and Excel files). There are even export and import wizards for Altium Designer.

It is even possible to use TRM with no layout data at all, for example, for preliminary placement studies or technological studies. The board will be calculated in three dimensions, even if desired as transient and with or without electrical sources (see the article by Doug Brooks in this issue). That will take between one and a few minutes. Much attention is paid to the user interface to have as much as possible in view at once, both in the input and in the results. It is truly easy to use and a teaching and learning tool for the EE (Figure 1).

Examples

In the first three examples, the value of the power dissipation is always 1 watt for the purpose of comparison, the PCB is always in "still air" (i.e., free convection), and the ambient temperature is always 20°C. Using the calculated component temperature, a thermal resistance "case-ambient" $R_{th,C-A} = (T_{case} - T_{amb})/1W$ can be read off directly. The fact that this value differs from board to board shows that also $R_{th,C-A}$ values in datasheets are not suitable for individual temperature predictions.

1. Arduino

The two-layer Arduino board is a standard Eagle [4] software installation. Solder mask and silkscreen do not need to be imported into the thermal model and are used here for illustrative reasons only. We only charge the central component IC3. Around the component, there is
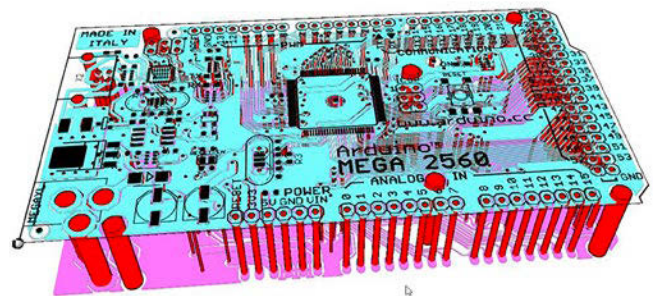

Figure 2: View of the TRM model of the two-layer Arduino board with solder mask and drilled holes. In the vertical direction, the geometry has been expanded by a factor of 10. The size is 100 mm x 53 mm. The components are hidden.

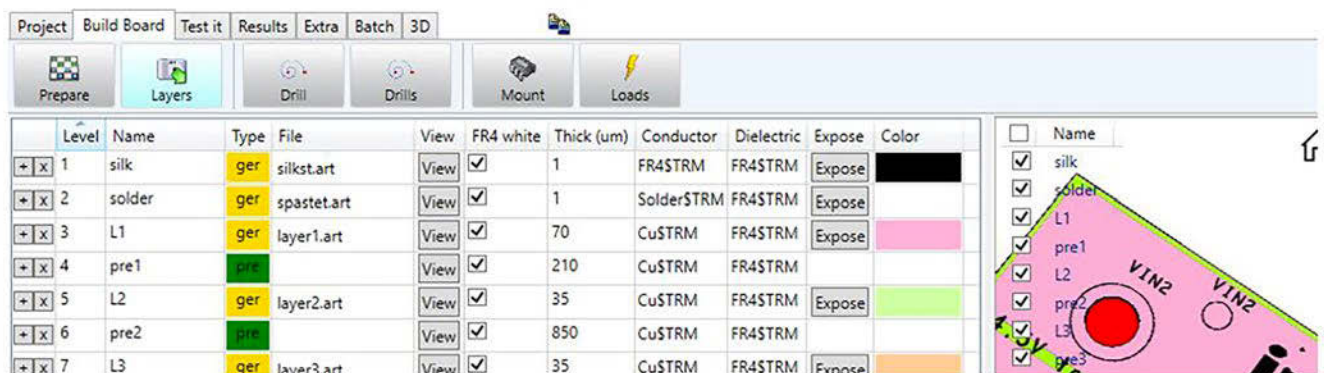|	Level	Name	Type	File	View	FR4 white	Thick (um)	Conductor	Dielectric	Expose	Color			Name
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+/x	2	solder	ger	spastet.art	View	✓	1	Solder$TRM	FR4$TRM	Expose			✓	solder
+/x	3	L1	ger	layer1.art	View	✓	70	Cu$TRM	FR4$TRM	Expose	🟪		✓	L1
+/x	4	pre1	pre			✓	210	Cu$TRM	FR4$TRM				✓	pre1
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+/x	6	pre2	pre		View	✓	850	Cu$TRM	FR4$TRM				✓	pre2
+/x	7	L3	ger	layer3.art	View	✓	35	Cu$TRM	FR4$TRM	Expose	🟧		✓	L3

Figure 1: The TRM user interface.

a nearly star-shaped arrangement of traces on top. With respect to the bottom, IC3 lies above a bundle of tracks surrounded by a flooded rest. Nevertheless, the cooling is not very good.

The calculated thermographs of the top and bottom are shown in Figure 2. The shape of the isotherms is very irregular, and the yellow and green sections end abruptly. The heat spreading does not manage to distribute the heat over a larger surface.

The reason can be seen illustratively if the temperatures are superimposed on the layout in the area around the component (Figure 3), the heat spreading ends where the gaps between the traces form an FR-4 barrier for the heat flow. This is not only true for the top layer, but also for the bottom. The overall result is then the superposition of the two structures (Figure 4).
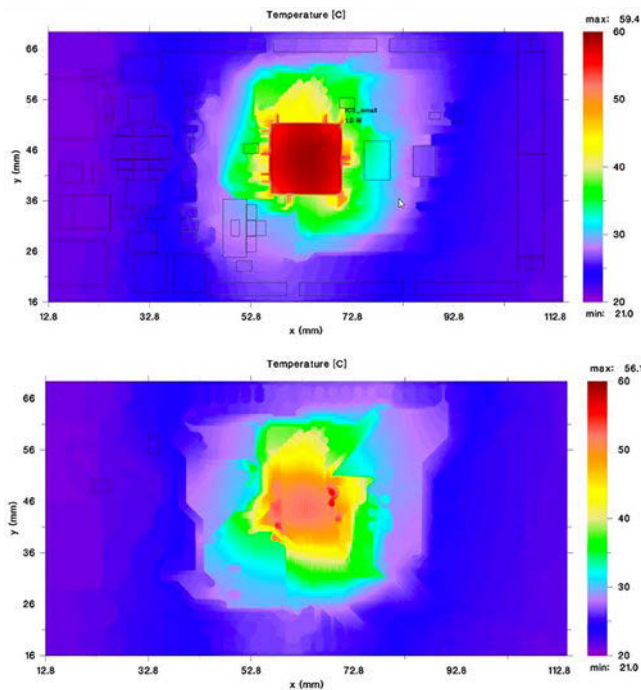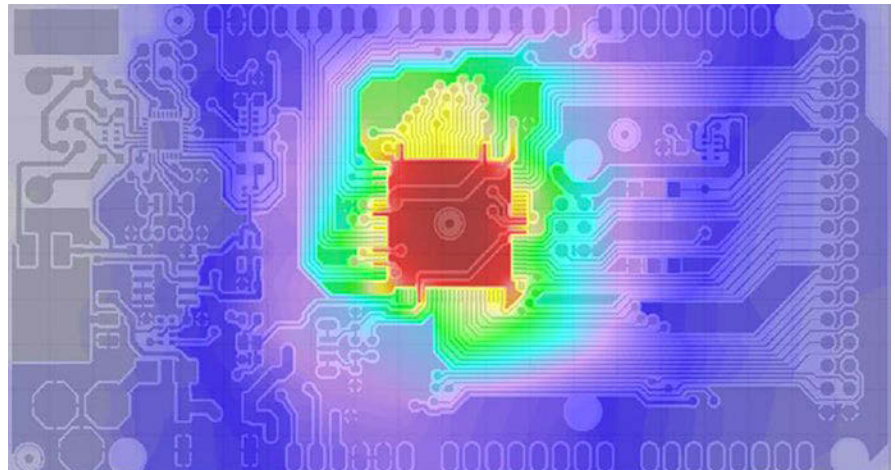

Figure 4: TRM calculated temperature field for the Arduino model with superimposed top-layer artwork. The parallel running traces can obstruct (left) or improve (above) the heat flow.

2. RS-ChipKit Max32

This board is a standard example of a DesignSpark PCB [5] installation. The four-layer board ChipKit Max32 by Digilent is a prototyping platform that demonstrates the power of the Microchip PIC32 microcontroller. The board is the same size as the Arduino board. On top and bottom, around the central microcontroller PIC32MX795F512L (= IC2), the tracks are orthogonally aligned like a woven pattern. Both inner layers are thoroughly flooded (Figure 5).

Because of the two massive inner layers, the shape of the calculated thermographs closely approximates that of circular isotherms from the theory of heat spread. The board is the same size as the Arduino, and even though the
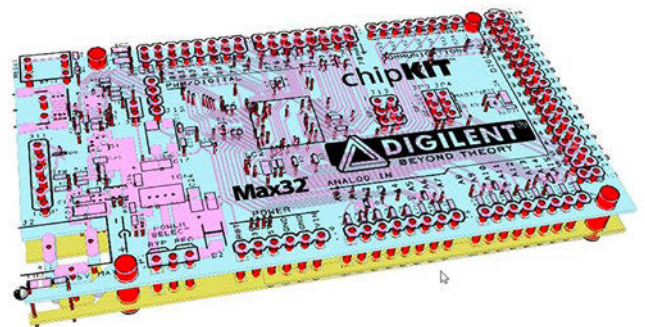

Figure 3: Calculated thermographs of the Arduino board for the top (above) and bottom (below). $R_{th,c-A}$ would be about 39 K/W.

Figure 5: Diligent evaluation board ChipKit Max32. The top layer in pink, first inner layer blue, and second inner layer in brown.
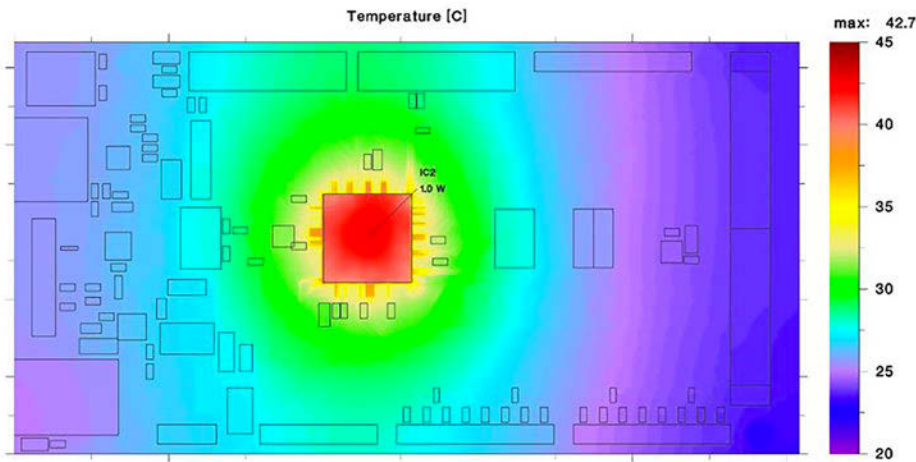
Temperature [C]   max: 42.7

Figure 6: Top layer temperature. Due to the two flooded inner layers, the isotherm is oval-shaped.

3. EVB-USB580x_A

This board is one of the standard examples of an Altium Designer [6] installation. EVB-USB5806 [7] is a demonstration and evaluation platform for the 6-Port SS/HS USB Smart Hub on a four-layer PCB. Below U1, there is a Cu pad that mates with the internal heat slug. The pad is only in contact with GND and can only dissipate heat there. In the Internal2 and Bottom layers, potential separations limit the heat spreading around U1 (Figure 7).

The result of the calculations is given in Figure 8. The circular isotherms on top are the result of the full surface copper in i1 (GND).

component is smaller, the temperature here is 20 K lower. This is the effect of heat spreading in the inner layers. Without the two inner layers, the temperature would climb to 80°C (Figure 6).
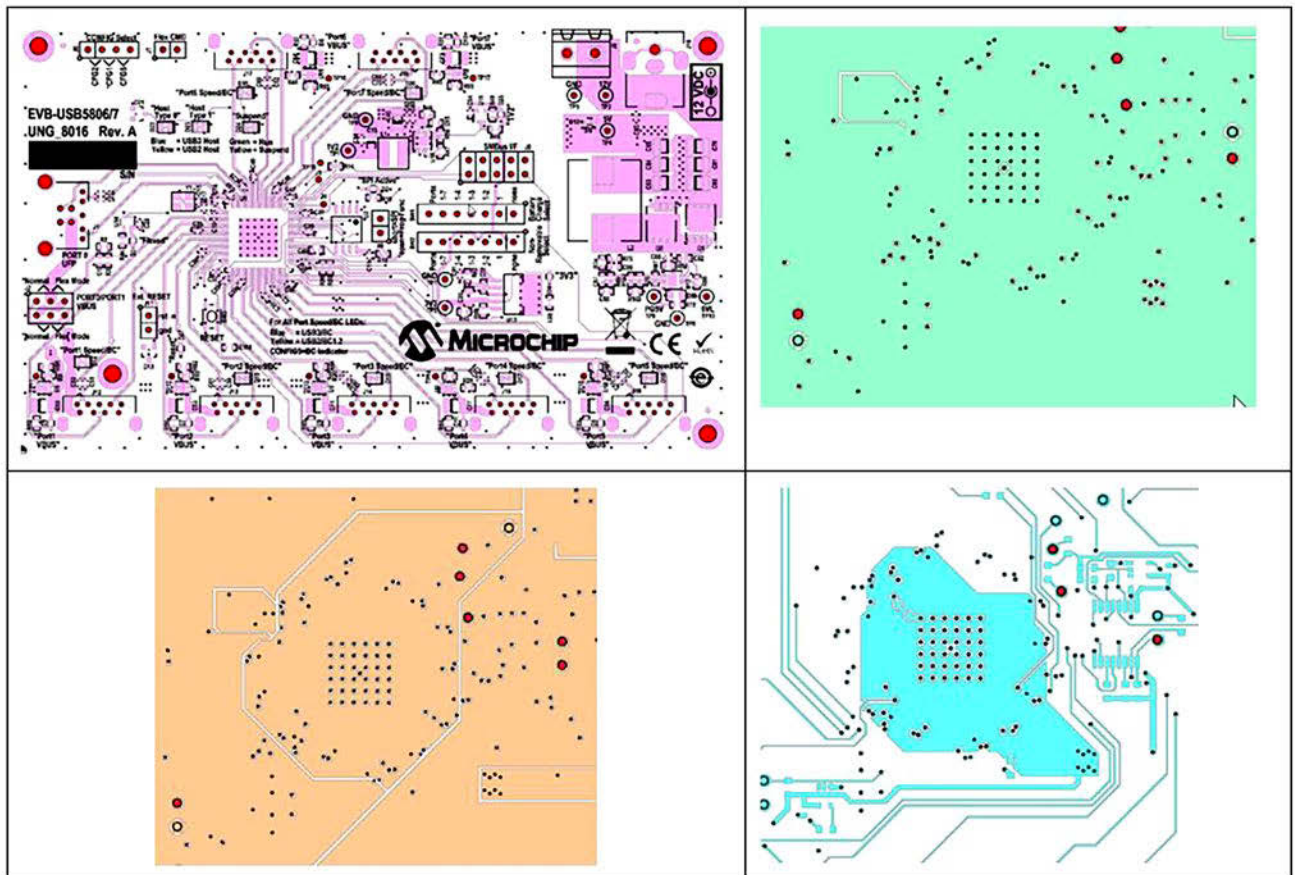

Figure 7: EVB-USB580x_A. General view of the top in pink, detail inner layer 1 (GND) green, detail inner layer 2 in brown, and detail of bottom in blue.
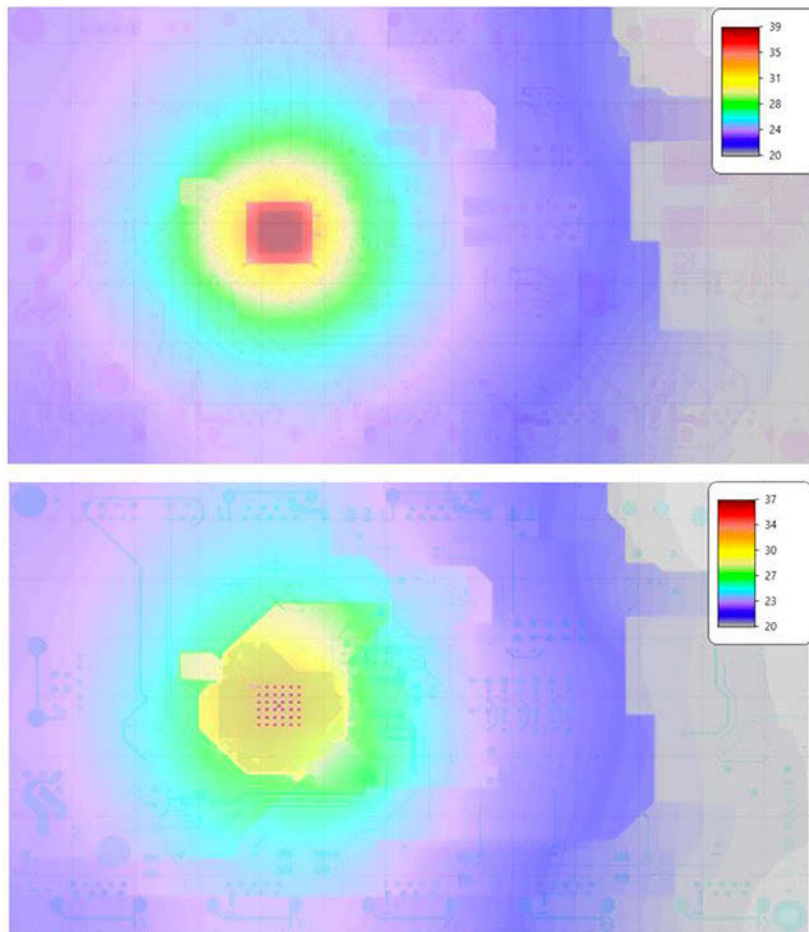
Figure 8. Calculated thermographs from the EVB-USB580X_A model superimposed on the layout images. The top layer (above) and bottom layer (below). The heat dissipation by PTH is poor.

But the geometrically limited heat spread in i2 and bottom impairs the temperature level. The rectangular pattern of red dots below U1 in the bottom layer is the PTH. They roughly show the temperature level of the component, not because they dissipate heat well, but because they dissipate it poorly and because the heat is in a dead-end. If the heat dissipation were good, the outer ring would have to be much colder. The one via in the upper left corner is an exception and is a customized construction on the bottom.

4. ISL8240MEVAL4: Comparison With Observation

Since there are infrared images and an article (Taranovich, 2015) [8] for the ISL8240MEVAL4Z [9] assembly, it is suitable for comparison with the simulation. The layout was created with

Cadence Allegro [10]. The comparison of simulation and experiment is very satisfactory (see details of the model [11]). Not only the maximum temperature is properly calculated, but also the edges and ridges caused by the layout of the inner layers are in their correct position. By the way, the "standard" method [12] is the wrong approach here (Figure 9).

Final Thoughts

Temperature also affects the electrical conductivity of the traces and the overall performance of the components ("derating") and the final product. (We intentionally omitted electric heating of traces in this article; see Doug Brooks' article in this issue. High-current applications in high ambient temperature can also be simulated with TRM, also as a mission profile with a time sequence of switching states). Early confidence that the components and traces will meet the temperature limits is one of the hallmarks of serious product development.

As the person responsible for heat dissipation, you can use the resulting graphs and tables (virtual thermographs) to clearly illustrate which actions are to be taken (or not) and why. Do not just believe that it will work out; you just have to want it and realize that good thermal design is cost-free. Even a prototype costs more money than just ordering the PCB sample online, and many bugged prototypes cost too much.

Our plea as a software provider is, of course, that thermal management should be accompanied by numerical simulation and that this should set the parameters for good solutions. But thermal management is also an interdisciplinary task because both the specifications and the solutions come from different directions. There is no panacea, and often, the development department is
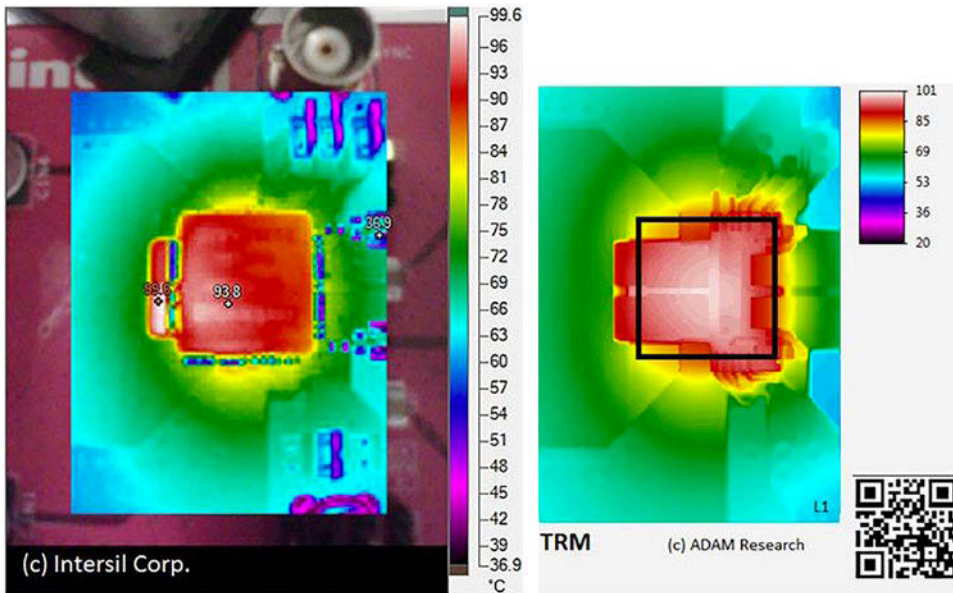
Figure 9: Thermography (left) and the simulation image of the top layer (right).

lab would be about 10 minutes until the steady-state is reached. Simulation can also be faster than real-time. **DESIGN007**

References
1. JEDEC.

2. Edwards, D., & Nguyen., H., "Semiconductor and IC Package Thermal Metrics," Texas Instruments Application Report SPRA953C, December 2003, Revised April 2016.

3. Wong, V., "Datasheet Intricacies: Absolute Maximum Ratings and Thermal Resistances," Analog Devices Technical Article MS-2251, 2011.

4. Eagle is a design software tool from Autodesk.

5. DesignSpark PCB is a design software from RS Components Ltd.

6. Altium Designer is a design software tool from Altium.

7. Microchip Technology, "EVB-USB5806 Evaluation Board."

8. Taranovich, S., "Unique Intersil thermal design removes heat from encapsulated, compact 50A power modules," 2015.

9. Renesas Electronics, "Dual 20A/Single 40A Step-Down Power Module Evaluation Boards," 2017.

10. Allegro is a design software from Cadence Design Systems.

11. Adam, J., & Jouppi, M., "Simulated and Experimental Component Temperature on the IntersilTM ISL8240 Evaluation Board," 2015.

12. Renesas Electronics, "Carrying the Heat Away from Power Module PCB Designs," 2018.

13. TRM is a thermal simulation tool for PCB from ADAM Research, adam-research.com.

caught between specifications, costs, design, marketing, reliability, and feasibility.

Think of the heat right from the beginning of development and communicate with internal and external development partners. Also, question any kind of estimate. "We have always done it this way" does not apply. Only reasonable communication can lead to a reasonable solution strategy.

It is impossible to predict when the ROI of a simulation software will be reached. For some users, this is already the case with the first project; usually, it should be the case with 2–3 development projects per year.

Unfortunately, electronics cooling is rarely offered as part of an electronics engineering university curriculum. TRM software can also be an educational tool. Even without importing layout data, you can create, calculate, and adjust a dummy with simple rectangles, circles or digital drawings. That is why TRM is also a prototyping and technology tool. You are free to choose the geometry, the layer structure, the materials, the thermal load by components and currents, and the cooling.

Since time is money, you should also know that the computing time, for example, with the ISL board, is about four minutes on my laptop. The duration of the measurement in the

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