

# Thermal Management of Boards and Current-Carrying Capacity of Traces

*An electrical current creates a local heat source in a trace - but board cooling is non-local*

*A three-dimensional, spatially detailed and combined simulation of electrical current and temperature in PCBs is the best approach to answer the question: “what is the maximum current for a trace at given temperature?” Board layout based on design rules IPC-2221 or IPC-2152 is merely a rough estimate leading to oversized traces or too conservative designs. We are discussing the effects of local heating and global cooling in a printed board and its consequence for temperature.*

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## Joule Heating

Electrical current in a wire causes deposition of thermal energy. To honour the discoverer of the effect, James Joule, it is called “Joule heating”. Nowadays Joule heating also plays an eminent role in electronics, e.g. for copper traces in printed circuit boards (PCBs). The thermal power  $P$  can be easily calculated using

$$P = R I^2 \quad (1)$$

where  $R$  is the electric resistance of the trace in Ohm and  $I$  the DC current in Ampere.  $R$  is a combination of geometric data (width  $w$ , height  $h$  and length  $L$ ) and material properties (specific electric resistance). Given  $w$  and  $h$  in mm,  $L$  in m and a value for copper at 20 deg C called  $\rho_{20}=0.0175 \text{ Ohm}\cdot\text{mm}^2/\text{m}$

$$R = \frac{L}{w \cdot h} \cdot \rho_{20} \cdot (1 + 0.00395 \cdot (T - 20)) \quad (2)$$

Two problems show up immediately:

Problem 1: What should be done, if the trace is geometrically not a wire cable?

Problem 2: How to write down a similar simple formula for the temperature  $T$ ?

The temperature of a trace in a PCB is the *result* of thermal equilibrium between Joule heating, conductive transfer of energy to other parts of the board, and convective / radiative *cooling* by the heat flowing from the board surface to the ambient environment.

Because of technological T-limits, like the glass transition temperature of FR4, the temperature of a copper trace must not exceed a certain value. A typical target used in industry is a maximum additional  $\Delta T_{\max}$  of about 20 K while all other components are off. Moreover the target depends on the ambient temperature.

## Simple Trace Temperature Estimates and Simulation

For first estimates the graphs in IPC-2221 (=MIL-STD-275) are widely used as a ‘design rule’ for trace geometry (i.e. trace width and height) for a given pair of current and temperature rise. For a reproduction and how to use them we refer to [1]. It may be doubted if this ‘standard’ is really useful and valid [2] anymore. First, layout experts

tell, that usually higher currents can be carried by a trace. Second, the IPC-2221 diagrams for so-called “internal conductors” are derated in current by a factor of two, exactly. These suspicious facts made it necessary to ask for further theoretical and experimental investigations.

While working on a revision of the old design rule, now called IPC-2152, the IPC Task Group 1-10b lead by M. Jouppi, found the root of IPC-2221 being experimental work for the National Bureau of Standards back in 1956 [3,4]. The original current vs. cross-section diagrams reproduced in [4] show a wide scatter of data points. This is due to the variety of investigated boards with different structure and coating. The final nomographs (i.e. Figure 1 in [1]) roughly represent the upper limit of the points. The lower limit is in close agreement with the so-called Design-News (‘DN’) correlations brought to notice by Brooks [2].

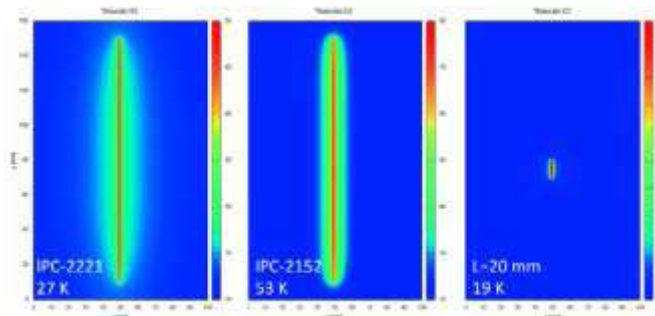


Figure1: Simulated thermographs of test boards with one powered trace ( $I=5 \text{ A}$ ). Left: a clad bilayer PCB rises to  $\Delta T=27 \text{ K}$  above ambient, middle: single layer PCB rises to  $\Delta T=53 \text{ K}$ , right: a very short trace on a bilayer can be cooler than a long trace because front and end face contribute considerably to cooling ( $\Delta T=19 \text{ K}$ ).

Questions: is it possible to explain or to reproduce the experimental IPC curves by numerical simulations? What could be learned? Could this technique be extrapolated to other scenarios? To answer the questions, we perform numerical studies on a simple 3-D model of a board using the author's software TRM [5] which is primarily designed to calculate complex multilayer layouts. The code is solving

numerically the partial differential equations of Ohm's law and Fourier's law to solve for high-resolution x-y-z distributions of potential  $U$ , current density  $j$ , Joule heating power density and temperature. Without knowledge of the exact NBS setup, we are assuming a model with a double-sided PCB in Euro-Format, with one copper trace of length  $L=100$  mm and of thickness  $h=35\text{ }\mu\text{m}$  ( $\approx 1$  oz) on the top face and a coated copper cladding on the back face (also of thickness  $35\text{ }\mu\text{m}$ ). In "still air" environment (parameterized by a heat exchange coefficient  $\alpha=10\text{ W/m}^2\text{K}$ ) the result for  $w=0.055"$  ( $\approx 1.4$  mm) and  $I=5$  A is shown in Fig. 1. The calculated maximum value of  $\Delta T=26$  K matches closely the blue line example in [1]. When the copper cladding on the bottom face is removed, the rise increases to  $\Delta T=53$  K, which is now very close to IPC-2152 and Brook's Design News data (59 K).

### Heat Spreading is Important

The examples in Fig. 1 show, that heat spreading in FR4 and by copper layers is essentially influencing the trace temperature. Having demonstrated the viability of the method, other layer stacks, although not detailed either, can be investigated. For example, a 4 layer board with 2 internal homogeneous copper planes (e.g. GND and VCC) has a much higher current carrying capacity than the IPC boards (Fig. 2). The calculated results [6,7,8] for other boards can be fitted by Eq. (3)

$$\Delta T \approx B_{PCB} \cdot \left(\frac{w}{\text{mm}}\right)^{-1.45} \cdot \left(\frac{h}{35\mu\text{m}}\right)^{-1} \cdot \left(\frac{I}{\text{Amp}}\right)^2, \quad (3)$$

where  $B_{PCB}$  is a characteristic figure for the board layer stack and layer parameters. Some values are given in Table 1.

| Layer Stack             | $B_{PCB}$ |
|-------------------------|-----------|
| DN and IPC-2152         | 3.6       |
| IPC-2221                | 1.7       |
| 2 internal 17mu planes  | 1.2       |
| 2 internal 35 mu planes | 1         |

Table 1: Coefficients for Current- Temperature Correlation Eq (3)

### IPC-2221 and IPC-2152 are not Universal

Eq. (3) reveals another drawback in both the old and new IPC charts. The horizontal axis shown there is the cross-section  $w \cdot h$  of the trace, which is incorrect. In fact the cross-section is controlling heating, but cooling is controlled by the footprint (width). This brings in another  $w^{0.45}$  term. Simulations also disprove the myth of hot internal traces:

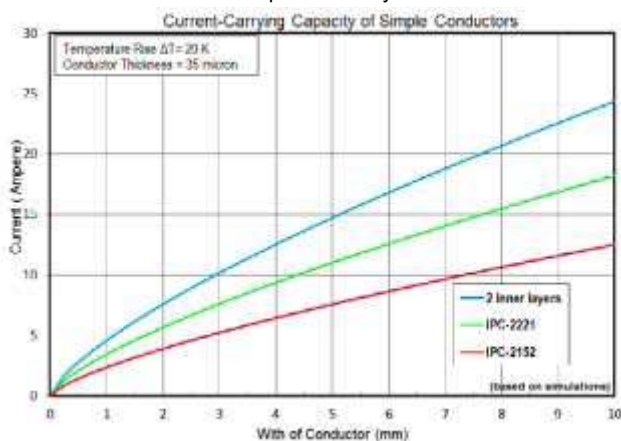


Figure 2: Current carrying capacity of a  $35\text{ }\mu\text{m}$  trace at temperature rise of  $\Delta T=20$  K. The more heat spreading, the more current can be carried.

an internal trace can be even cooler than an external trace, because of better heat spreading above and below. Finally we should mention that the new IPC-2152 values are close to "DN" correlations and is therefore more conservative than the old 2221.

### High-Resolution 3-D Multilayer Simulations

Eq. (3) does not contain the trace length  $L$ , because  $P$  and the area of left and right cooling wings are proportional to  $L$ . However this is true only for long traces. From Fig.1 (left) we can estimate a width of the wings of about 10 to 20 mm. In this model a trace may be called short, if  $L < 20$  mm. If we now simulate a trace with  $L=10$  mm (Fig. 1 right) we see that the result  $\Delta T_{\max}=19$  K does not agree anymore with Eq. (3).

Realistic layouts are more complex and hence are the genuine application for numerical simulation. We can observe current concentrations at *constrictions*, *curvature* effects and *shielding* of current by other conductors. Fig. 3 shows a close-up of results of a calculation with x-y resolution of 0.1 mm. We assume a bilayer PCB like in IPC-2221. Current of 18 A enters each conductor path via 3 pins at 6 A each and leaves by 4 pins terminated to 0 V. Fig. 3 (top) shows the potential (with potential lines), the current density and the temperature in a layout *with thermal reliefs*. The middle conductor has the lowest cross section and thus the highest DC voltage drop (31 mV). It is also the hottest ( $\Delta T_{\max}=20$  K), because it is surrounded by two other heat sources. The current density is related to the potential gradient and forms characteristic patterns: high values between pins with shortest distance, in constrictions and at inside bends, and low values around "shielded" pins and outside bends. The thermal conductivity is high enough to smear out the local heating effects. Fig 3 (bottom) shows the same situation *without thermal reliefs*. Now, maximum voltage drop is 27 mV and  $\Delta T_{\max}$  is 18 K. Don't try to predict these temperature with design rules!

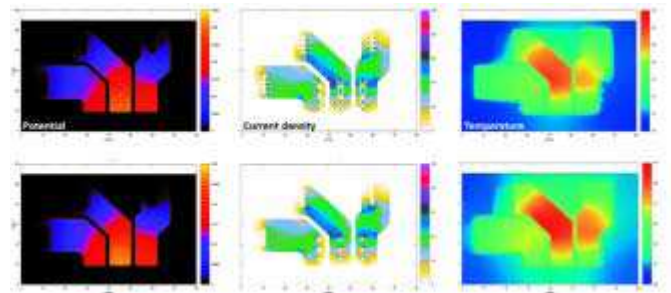


Figure 3: Consistent high-resolution simulations of three conductor paths at 18 A each. Top: with thermal reliefs, bottom: without reliefs (scales are individual).

### References:

- [1] [http://www.ultracadm.com/using\\_ipc\\_temp\\_charts.pdf](http://www.ultracadm.com/using_ipc_temp_charts.pdf)
- [2] Brooks, D., <http://www.ultracadm.com/articles/pcbtemp.pdf>
- [3] Jouppi, M. R., "Thermal Characterization of PCB Conductors", Electronics Circuits World Convention 9 Cologne, 2002.
- [4] [www.ipc.org](http://www.ipc.org) → IPC-2152 or [www.fed.de](http://www.fed.de) → IPC-2152
- [5] [www.adam-research.de/TRM.html](http://www.adam-research.de/TRM.html)
- [6] Adam, J., "New Correlations Between Electrical Current and Temperature Rise in PCB Traces" Proc. 20th IEEE SEMI-THERM Symposium, 292-299, 2004.
- [7] Adam, J., "Neues von der Strombelastbarkeit von Leiterbahnen" GMM Fachbericht 44 „Elektronische Baugruppen“, 117-123, 2004.
- [8] Adam, J.: „Strombelastbarkeit von Leiterbahnen III. Weitere Diagramme für Multilayer und Umrechnungsregeln“, PLUS 6, Heft 4 S. 513, 2004.