TRM Case Study No. 2

Electric Current and VIA Temperature – Experiment vs. Simulation

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INTRODUCTION

In discussion forums we find questions about how to size vias (vertical interconnects). What would be a good drill hole diameter so that a given electric current would not overheat (Joule heating) and lead to mechanical damages in the PCB? IPC-2152 recommends that the plated ring area in the via should be roughly equal to the cross-sectional area of the joint traces. To get answers, experiments are needed. This note is based on the initiative of D. Brooks and the experimental results of his work [1, 2]. J.A. compiled the modeling with TRM[1] and recalculated the simulation results.

THE MATERIAL

The following paragraph from Brooks [1] describes the experimental setup. "The relevant portion of the test board is shown in Figure 1. The board is approximately 60 mils thick "FR4".The board contains 0.5 Oz. copper nominally plated with 1.0 Oz. additional copper. Two traces were compared, one nominally 27 mils wide, the other 200 mils wide. Each trace is 6.0" in length, one-half on the top layer and one-half on the bottom layer. Each trace has a single 10 mil diameter plated via connecting top to bottom. It is important to note that the via structure is identical in each trace. The board was supported 2.5 inches above a plywood surface in still air by four screws at the corners. The board was micro sectioned after testing to measure the actual dimensions for the simulation. The thicknesses were (top layer) 2.1 mil and (bottom layer) 2.9 mil".

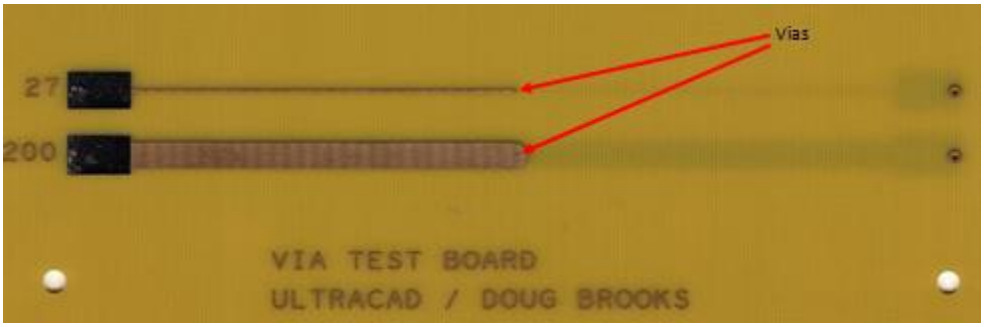


Figure 1: The board under consideration [1]. Size of this portion is 165 mm x 53 mm.

[1] TRM= "Thermal Risk Management in Electronics" is software by ADAM Research [3].

EXPERIMENTAL RESULTS

Thermocouples were placed approximately 2/3 of the way between the pad and the via. For each test, a constant current is applied to the trace until the temperature stabilizes (approximately six minutes.) Then the temperature is measured and recorded [1]. Table 1 reports the results for a room temperature of 25 °C.

Table 1 Measured Test Results

	(1)	(2)	(3)	(4)	(5)
	Trace width (mils)	**Current (A)**	**Trace Temp. (°C)**	**Via Temp. (°C)**	**Via ΔT/Trace ΔT**
(a)	27	4.75	66	64.5	0.96
(b)	27	6.65	114	109	0.94
(c)	200	4.75	30.5	31.5	1.2
(d)	200	8.55	40.5	44.5	1.3

There is one especially important observation that should be made here [1]:

- a 6.6 Amp current through the 27 mil wide trace results in a via temperature of 109 °C
- while a *higher* current of 8.6 Amps results in a larger (200 mil wide) trace results in a ***much*** *lower* via temperature of only 44.5 °C.

This confirms that it is the trace that is controlling the via temperature!

BOARD MODELING

[1]: "An important parameter in any thermal model is the thermal conductivity for the dielectric. Rather than trust the estimates on the Web and the sometimes incomplete measures found on data sheets, a sample of board material was sent to C-Therm in Canada. They measured the thermal conductivities as (W/mK):

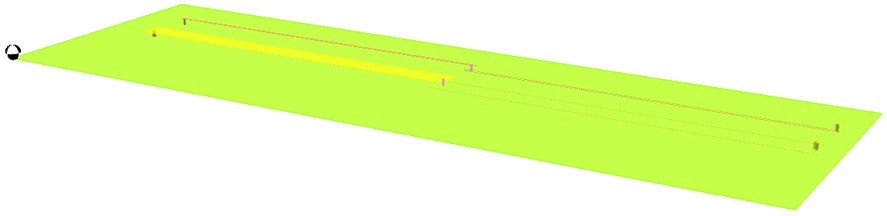
- In-plane: 0.679 W/mK
- Through-plane: 0.512 W/mK"

These values are a mix of polymer (0.2 to 0.3 W/mK) and (woven) glass fiber (1 W/mK) conductivity.

Applied board size of the model is 165 x 53 mm. The finest structures in the layout are around 0.1 mm. This is the lateral resolution which we demand for the results.

Level	Name	Type	File	View	FR4 white	Thick (mu)	Conductor	Dielectric
1	top	pre		View	☑	53		DougTraceBoard
2	core	pre		View	☑	300		DougTraceBoard
3	center	pre		View	☑	900		DougTraceBoard
4	core	pre		View	☑	300		DougTraceBoard
5	bot	pre		View	☑	73		DougTraceBoard

Fictitious "Layer stack" in TRM. To create a little finer discretization of the inner part in *z* the plate was divided into 3 sub plates. This does not have much influence on the results. Traces are plced in "top" and "bot"



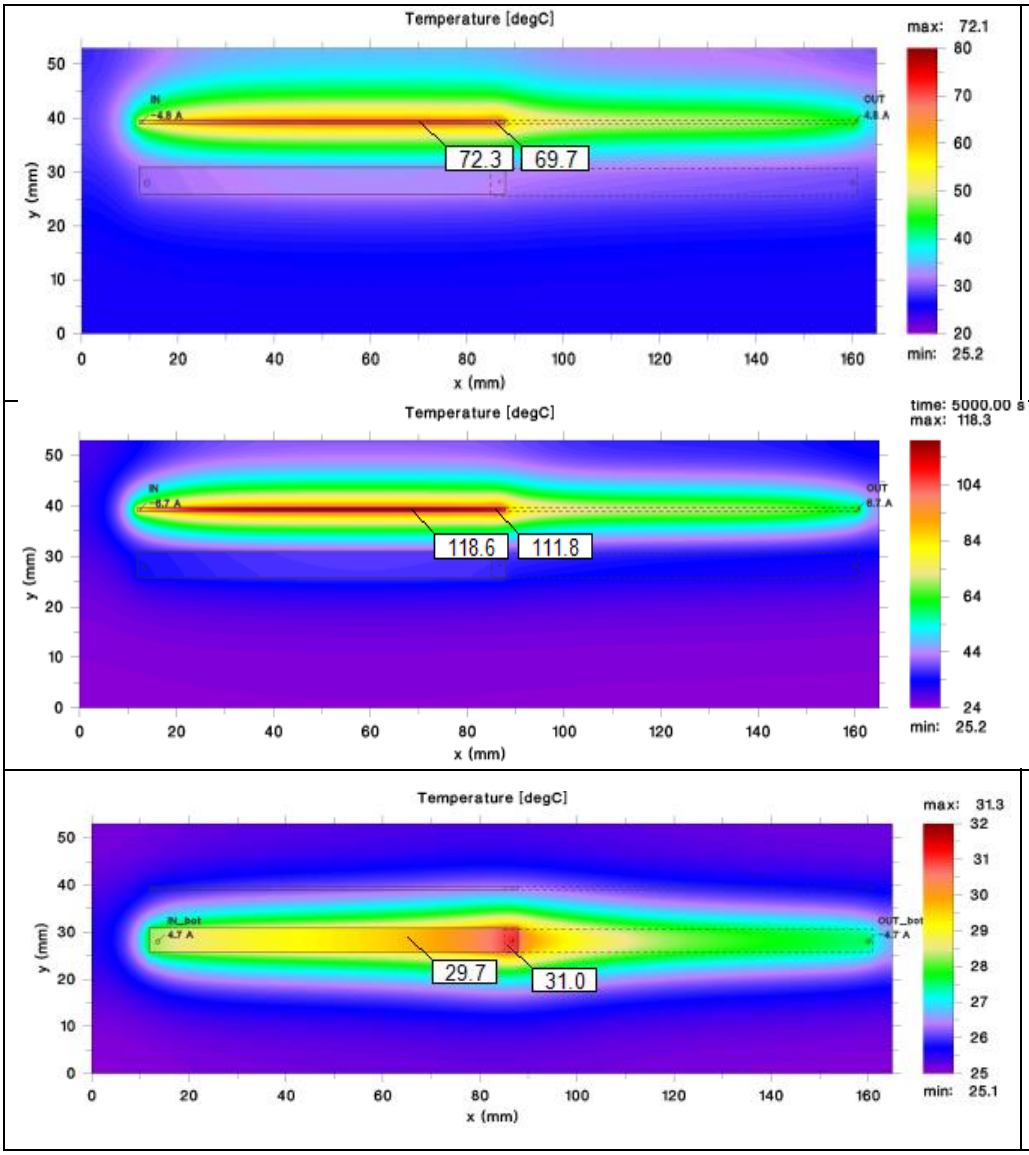
Transparent 3D view of our board model. Bottom traces (left) are dashed.

Figure 2: Summary of the model-build in TRM.

Fig. 2. has a perspective view of the traces with the substrate. The outermost cylinders are pins to supply and extract electricity. The central cylinders are interconnects (vias).

SIMULATION RESULTS

Fig. 3 shows the simulation results for the lines in Table 1. The simulated "virtual" thermo-graph of the top layer is shown. The temperature labels approximatively coincide with the position of thermocouples in the experiment. The Joule power dissipation of the traces + via is indicated.



(a)

27 mils / 4.75 A

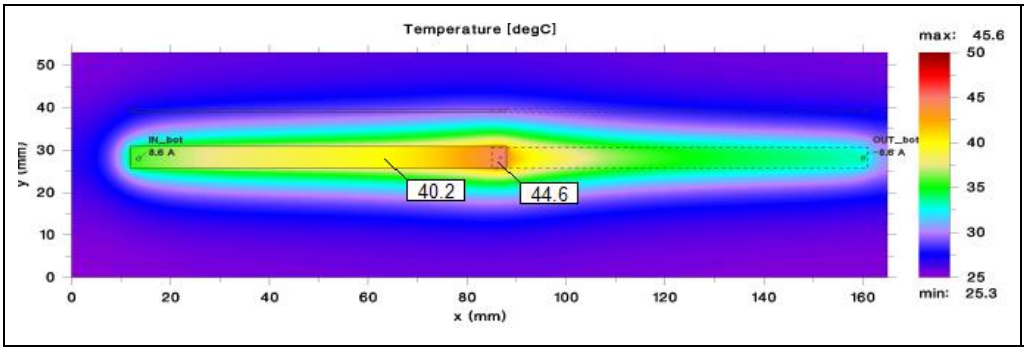
(b)

27mils / 6.65 A

Convection and radiation sepa-rated.

(c)

200 mils /4.75 A



(d)

200 mils /8.55 A

Figure 3: Simulated temperature of the top layer

The heat transfer coefficient *h* was taken from flat plate correlations in a free convection environment (taking into account the individual power loss and with deliberate additional little turbulence) plus a plate averaged radiative contribution with a surface emissivity of 0.95. For the wide trace the agreement between experiment and simulation is extremely good. For the narrow trace in Fig. 3b this (standard) procedure would lead to 20% too high values. However, if we separate convection from radiation, i.e. use a plate averaged convective *h* plus a local T^3 radiative *h*, the hotspot cools comparably better and agreement is now close to the experiment. We used the standard textbook electric resistivity data for pure copper ($\rho_{el,20}$ = 0.0175 Ω•mm²/m, α_{20} = 0.00395 1/K).

DIAGNOSIS

Table 2 contains more diagnostic values:

Col. (6): Joule heat in the model as derived from calculated current density

Col. (7): Portion of Joule heat inside the via

Col. (8): The simulated top traces temperature without a central via.

Col. (9): Adopted heat transfer coefficient.

Table 2. Simulated temperature and more diagnostic values

	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)
	Trace width (mils)/(mm)	**Current** (A)	**Trace Temp.** (°C)	**Via Temp.** (°C)	**Via ΔT / Trace ΔT**	**Total power** (W)	**Power in via** (W)	**Trace temp without via** (°C)	Adoptd. ***h*** (W/m²K)
(a)	27 / 0.7	4.75	72	70	0.95	1.6	0.03	72	12
(b)	27 / 0.7	6.65	118	112	0.94	3.6	0.10	114	$8+h(T^3)$
(c)	200 / 5.1	4.75	30	31	1.2	0.24	0.03	29	11
(d)	200 / 5.1	8.55	40	45	1.3	0.77	0.06	38	11

To distinguish the interaction of the via with the trace, we calculate additional board models without vias and without traces.

For the first type of models we place two additional pads to terminate the top and bottom trace individually and remove the vias. The calculated thermographs for the narrow 27 mils traces *without* vias look very much as in Fig. 3a,b. The temperature distribution of the wide trace shows a characteristic difference: the spot of maximum temperature moves from the via to the midpoint of the trace (Fig. 4). This agrees with previous arguments that the ends of a trace always are cooler than the center.

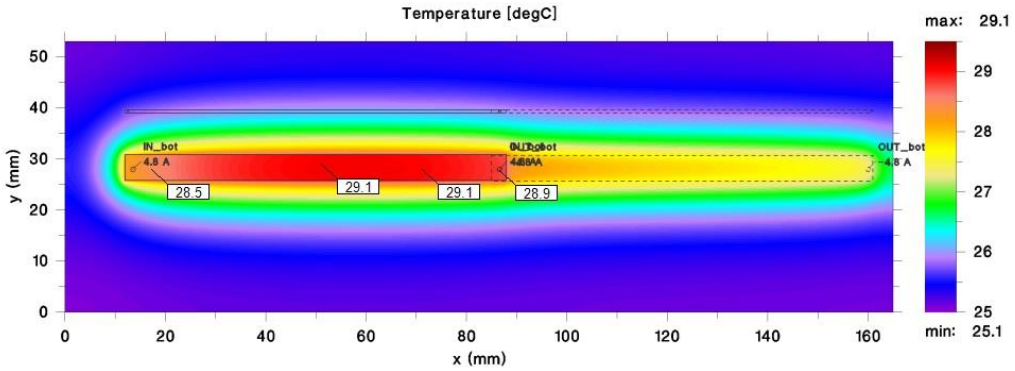


Figure 4: Simulation result of 200 mils & 4.75 A with 2 separate traces without interconnect.

For the second type of models we place pads at the top and bottom end of the via and remove the traces. Relative to ambient the via column is about 3 times hotter (Fig. 5) than with traces (Fig. 3). *This proves the proposition that the via is cooling into the trace.* It also explains why the influence of the via is neglegible for the 27 mil traces. *This is because this trace is hotter than the via.*

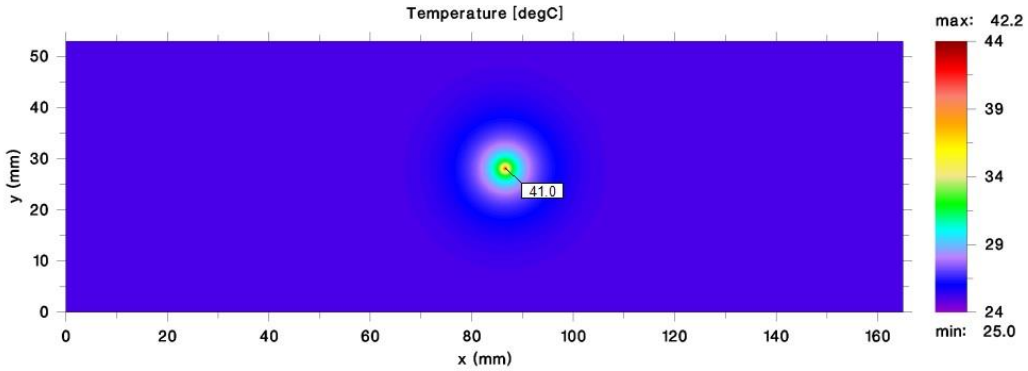


Figure 5: Simulation result of 4.75 A through the interconnect without traces.

The no-via calculations can explain the transition of Via ΔT/Trace ΔT from <1 to >1 from the small to the wide trace. At 20 mils the power dissipation in the via is negligible but the via is adding some area to shovel heat into the dielectric. In the wide trace the via contributes 10% to Joule heat and this extra is conducted away from the via onto the trace, resulting in the via being a little hotter (but not a LOT hotter) than the trace.

CONCLUSION

In opposition to general believe it is not the current that determines the temperature of a via, it is the temperature of the associated traces. This invalidates any estimates of via tempera-

tures merely from Joule heat values. For a printed board in a real world application a three-dimensional co-simulation of current and temperature [3] is required.

More discussion about trace sizing can be found in [2]. If the traces are sized correctly for the current level, *MUCH* smaller, and fewer, vias are required to transition between trace layers than has been previously believed. This means designers can have much greater flexibility in freeing up routing channels underneath the traces on their boards.

ACKNOWLEDGEMENTS

C-Therm Technologies (Fredericton, New Brunswick) graciously measured the thermal conductivity of the board material to facilitate the simulation. And a special thanks to Prototron Circuits, Inc. (of Redmond, WA) who provided the test boards and also the micro-sectioning work and measurements.

REFERENCES

[1] Brooks, D.: “Empirical Confirmation of Via Temperatures“, *Printed Circuit Design & Fab Circuits Assembly* http://www.pcdandf.com/pcdesign/index.php/magazine/10604-thermal-modeling-1602. in print (2016)

[2] Brooks, D., Adam, J.: “Via Currents and Temperatures”. http://ultracad.com/articles/via.pdf (2015)

[3] Adam, J., “Thermal Risk Management”. http://www.adam-research.de/index.php?seite=trm&lang=eng (2010)

