White Paper No. 11
The Junction Temperature

Question: Can TRM deliver the junction temperature of a component?

1 Introduction

An easy question, but to give a very precise answer needs some deep knowledge of heat transfer and much of package details. In this case, an engineers' approach is required and in this paper we shall focus on simplicity.

The treated part of the surface of the silicon die inside a component package is commonly called the "Junction". This is where the switching operations are done and where the heat is produced. The junction must not exceed some specified temperature otherwise the package is damaged and it will fail. The junction temperature not only depends on the dissipated power but also on heat removal (heat spreading) by conduction in the local layout around the component and the other materials in the board. This effect makes it difficult to compare simulation with experiments when the experimental board layout details are unknown.

To show a solution we discuss a package be of type SOT-23

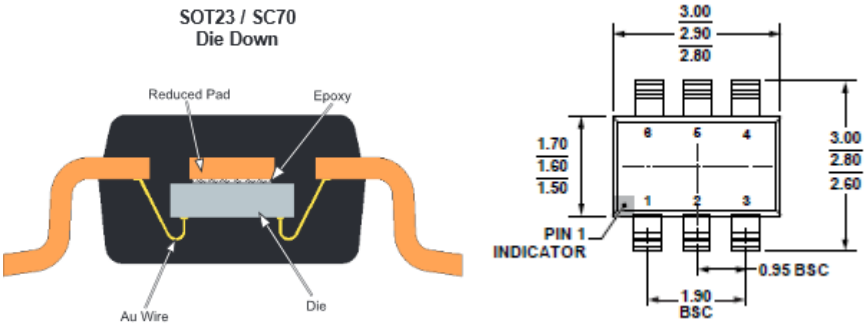


Figure 1: SOT23 (Sources: left: http://www.amkor.co.kr/datasheets/SOT_SC.pdf right:Analog Devices)

The simplest approach with TRM is to create a board model, to place a quad-shaped component and to run with a test power. The reported temperature of the component body should then be interpreted as being "close to the board temperature underneath the component". Our model board is imitating a single-sided JEDEC-51 low thermal conductivity test board having some traces but otherwise no extra copper.

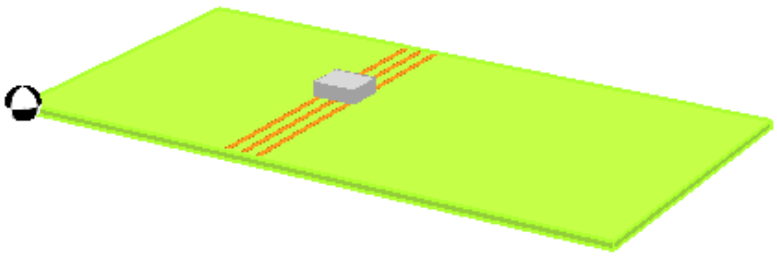


Figure 2: TRM model of a low conductivity test board

The result of the TRM calculation using a test power of P=0.1 Watt is around T_C≈50 °C under free convection at room temperature.

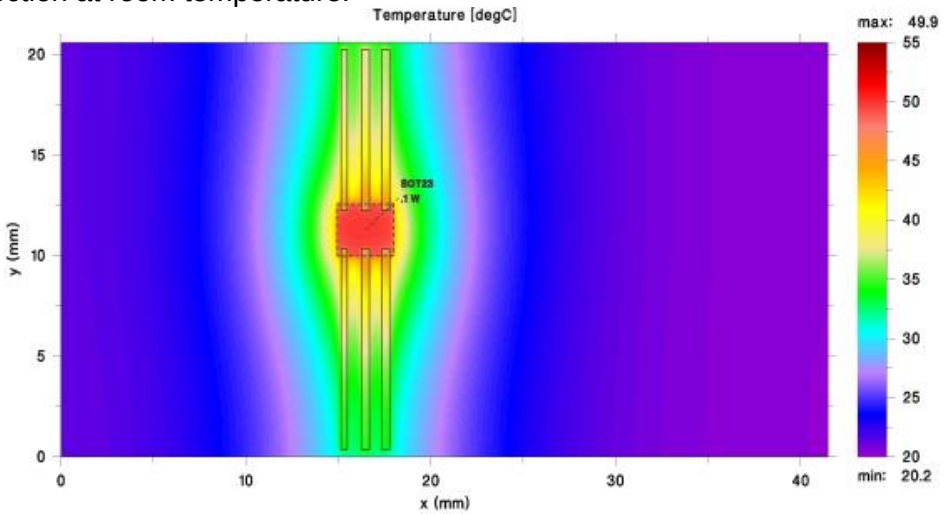


Figure 3: Result on a test board using 0.1 Watt and a heating area of 3 x 2.6 mm

If (and only if) we can assume that this temperature is an approximation to the case temperature we use additional package information from the manufacturer: the thermal resistance from case ("C") to junction ("J") and case to board ("B") (or junction to board in combination). For example Analog Devices publish a J-C thermal resistance of 90 K/W:

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 11. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
6-Lead SOT-23 (RJ-6)	230	92	°C/W

Figure 4: Some data sheet (source: Analog Devices: ADR3412/ADR3420/ADR3425/ADR3430/ADR3433/ADR3440/ADR3450 (Rev. B))

We multiply this thermal resistance by power and get a temperature difference between case and junction $\Delta T_{J\text{-}C}$ =90 K/W*0.1 W = 9 K. If we add this to the supposed case temperature from Fig. 3 a junction temperature results around

$$T_J = T_C + \Delta T_{J\text{-}C} = 50\ °C + 9K \approx 60\ °C.$$

The careful reader will recognize that the thermal resistance J-A in the data sheet is 230 K/W which, multiplied by 0.1 Watt, leads to a junction temperature of 20 °C + 230 K/W*0.1 W = 43 °C. This is lower than the calculated case temperature on our test board and illustrates the uncertainties and the complexity of the problem. Only additional information about the layout and the thermal resistance between board and package can lead to a reliable result. In that case the package manufacturer must assist.

2 Approximation

There is another approach to the junction temperature, if we know the so-called "2-Resistor-Network" of the package.

These values are called $R_{J\text{-}top}$) and $R_{J\text{-}board}$) and they provide the values for TRM's loads table' cells K/W-air and K/W-board K/W-board K/W-air . In order not to add artificial resistance from the component material the TRM component should then get a high thermal conductivity (e.g. copper). The temperature then shown in the result pictures and tables will be T_J (or something close to it) instead of a "close to board" temperature.

The physics behind the concept is well described in Texas Instruments' Design Guide http://www.ti.com/lit/an/sprabi3/sprabi3.pdf and in JESD15-3 (www.jedec.org) .

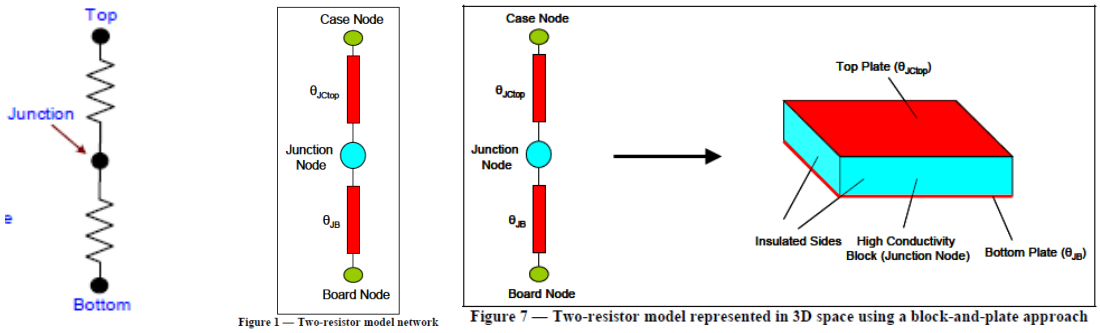


Figure 5: 2R network representations from TI (left) and JESD15-3

"Junction" is the center of the representing component brick in TRM, "Top" is the top face towards air and "Board" the bottom face towards the board. Everything happens virtually inside the component. If we knew the values of the two resistors, T_J can be calculated. But the approach is not unproblematic at all, which we see in the example below. The best representation is achieved if one of the 2 resistances is infinitely large, so that the heat flow is unidirectional. In that case the total power can be multiplied by R. Otherwise partial heat fluxes have to be applied which is a difficult task with a pocket calculator.

Don't mix up $R_{J\text{-}top}$ with $R_{J\text{-}ambient}$: the 'ambient' value from data sheets is not usable in a real application context (only for crude estimates on a pocket calculator), because $R_{J\text{-}ambient}$ intrinsically contains the interaction of the package with the test board and its layout. To calculate this interaction (heat spreading) is just the task for a TRM calculation and we should not mix it. Be aware that the test boards in JEDEC are of low copper content and presumably not comparable to a real application. There are more complicated package networks, but to get those values is more difficult and they are not implemented in TRM.

3 Values

Where to get the thermal resistance values? This is often difficult, because data sheets do not tell all necessary details or show sugarcoated numbers. R_{JC} can often be found, but the geometric position of 'case' should also be well defined (which rarely is the case). R_{JB} is less frequently published because it is extensive. The method being recommended to determine R_{JB} by the JEDEC JC15.1 committee uses a cold plate in a "ring" or "window frame" configuration clamped on both sides of the printed circuit board with the top of the package and the bottom of the board insulated. Mentor Graphics offers a calculation tool called FloPack where lots of geometric and material data can be placed into package data templates and as the result the thermal network comes out.

But a good package manufacturer should be able to tell us the values - on request.

Let us make a little survey and show examples based on the website of Analog Devices ("AD"). The basics and definitions are described in their MT-093.pdf (http://www.analog.com/media/en/training-seminars/tutorials/MT-093.pdf)

AD only knows about $R_{J\text{-}Ambient}$ and $R_{J\text{-}Case}$ and they give as a rule $\theta_{JA} = \theta_{JC} + \theta_{CA}$ (Theta and *R* are almost equivalent, but there are some academic differences in their definitions). The temperature of the Junction then should be estimated from $T_J = T_A + (P * R_{JA})$. In a complementary doc AN-892.pdf we find these pictures,

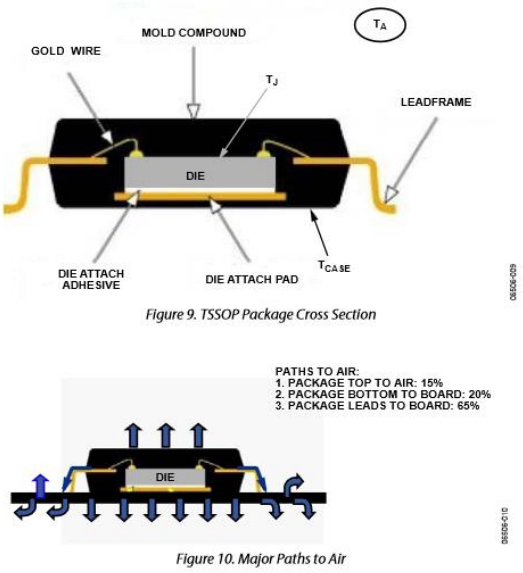


Figure 6: Some inner life of a package

Analog Devices (MT-093.pdf)

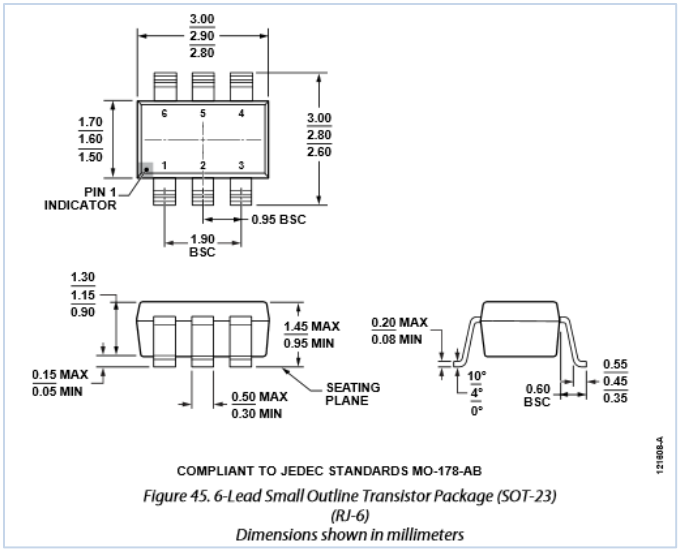
which show the difficulties caused by the individuality of components: the geometric spot, where 'case' is defined can be either the bottom face or the top face of the component. This depends on the internal construction of the package and where the heat flow is conducted to. Some components are designed to cool towards the board (presumably done in Fig. 6) and others are designed to cool to a heat sink on the top surface. This individuality has to be found in the data sheets and taken into account when using values for TRM.

4 Elaborate example SOT23

4.1 Package data

Each manufacturer has its own techniques and materials to build-up the internal structure of a package. The name of the package, like SOT23, only defines the standardized outline.

We now summarize the result from AD's website (www.analog.com) for the values for SOT23. The info that the die is 'down' means that cooling should be managed from the board side and not by a heat sink attached on top.



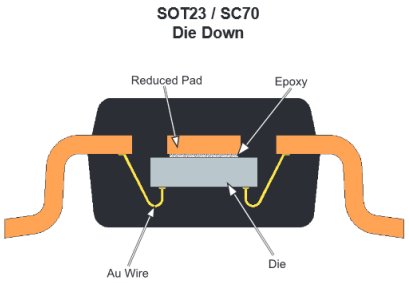


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Table 11. Thermal Resistance

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6-Lead SOT-23 (RJ-6)	230	92	°C/W

Figure 7: Collection of data on SOT23 from Analog Devices

At first glance we can assume that J-C is defined between die and bottom, because it is unlikely that a heat sink should be mounted on top of the package.

How reasonable are the values? Amkor gives this data sheet without J-C values where the JA values are a bit larger for a single layer board and a bit lower for a board with 2 internal planes. We see that the values for SOT23 are not 'universal material data', but contain manufacturing details and their margins.

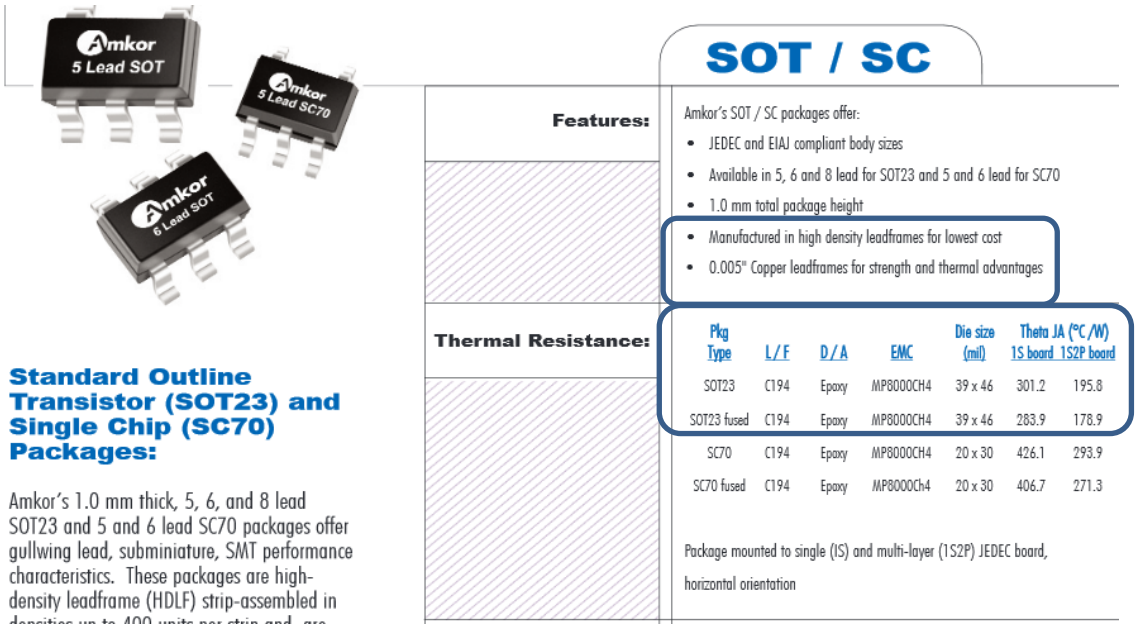

Figure 8: Source: http://www.amkor.co.kr/datasheets/SOT_SC.pdf

4.2 Some checks

First, we make a check for the bulk thermal conductivity. We use the definition of the thermal resistance of a 1D thermally insulated slab: $R_{\text{th}} := \frac{d}{k \cdot A}$, where d is the distance of heat flow, *k* the conductivity of the slab and *A* the area of heat flow. We solve this formula for *k* by using as an area the footprint which is about *A*≈3 mm * 2.6 mm, heat travelling distance *d*≈1 mm and R_{th}=92 K/W. The resulting value for the bulk thermal conductivity *k* is around *k*≈1 W/mK.

This value is quite reasonable and reflects the fact, that the package is ‘simple’ and has little metal content inside.

Second, we try to retrieve some value for the effective heat exchange coefficient *h* - from the surface to ambient - using the relation $R_{th}=1/(h \cdot A)$. We take $R_{th}=R_{CA}$, the case-ambient resistance, which is about 230-92 K/W=140 K/W and get some $h \approx 1400$ W/m²K, which is a very large and strange value. However, we made an error in assuming the area of convective heat transfer *A* to be the top face area of the component only. From our experience, the diameter of the hotspot on a 2-layer test board is of the order between 20 mm and 30 mm, thus it is also the surrounding PCB material which is cooling the package and not the package surface alone.

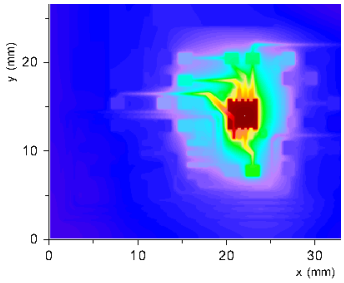

Figure 9: A typical heated halo around a component.

If some assumed 30mm x 30mm halo contributes substantially to heat transfer to the ambient, then $h \approx 1/(140 \text{ K/W} * 0.03 \text{ m} * 0.03 \text{ m}) \approx 10$ W/m²K which is indeed in the range of typical free convection values. The air gap between package bottom face and board is another awkward detail which we will now ignore but which could be important.

We learn that the numbers are reasonable but have to be taken with care and things are not that easy.

4.3 TRM modelling

Which TRM modelling to recommend for this package? Perhaps this one:

Name	Posx (mm)	Posy (mm)	Dimx (mm)	Dimy (mm)	Height (mm)	z-Begin	z-End	Material	Form	K/W-board	K/W-air	Watt
SOT23	15	10	3	2.6	1	0	0	Cu$TRM	r	90	-1	0.1

Deliberately we use a power of 0.1 Watt and used copper as the component material in agreement with Fig. 5 rhs.

Unfortunately we do not know the test board used for the data sheet values, but typically is has a low copper content.

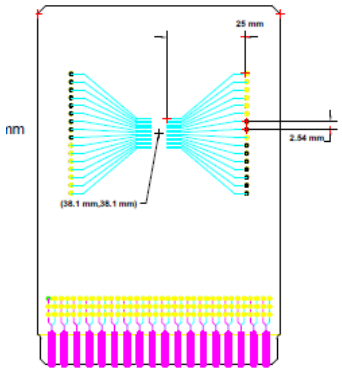

Figure 5 — Traces flared to 2.54 mm centered vias @25 mm from package body

Figure 10: low-conductivity-board layout from JESD51-7

The layout in Fig. 10 is not available to us in Gerber format. Therefore we assume some average conductivity of around 3 W/m-K of the layout pattern and a layer stack-up like this

Level	Name	Type	File	View	FR4 white?	Thick (mu)	Conductor	Dielectric
1	top	pre		View	☑	35	Cu$TRM	k=3$TRM
2	core	pre		View	☑	835	Cu$TRM	FR4$TRM
4	core	pre		View	☑	835	Cu$TRM	FR4$TRM
5	bot	pre		View	☑	35	Cu$TRM	FR4$TRM

The TRM result for a power of 0.1 W is 77 °C:

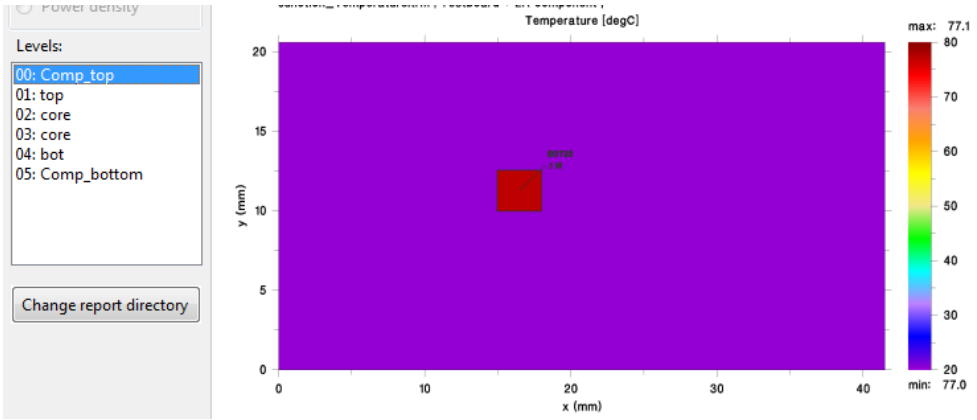

Figure 11: Calculated „junction“ temperature of a 2R component model on a test board

Why isn’t the component temperature equal to 20 °C + 90 K/W*0.1 W=29 °C?

Because the resistance R_{JC} is not connecting Junction with ambient temperature 20 °C but Junction with board layer temperature. The thermal map of layer 1 is

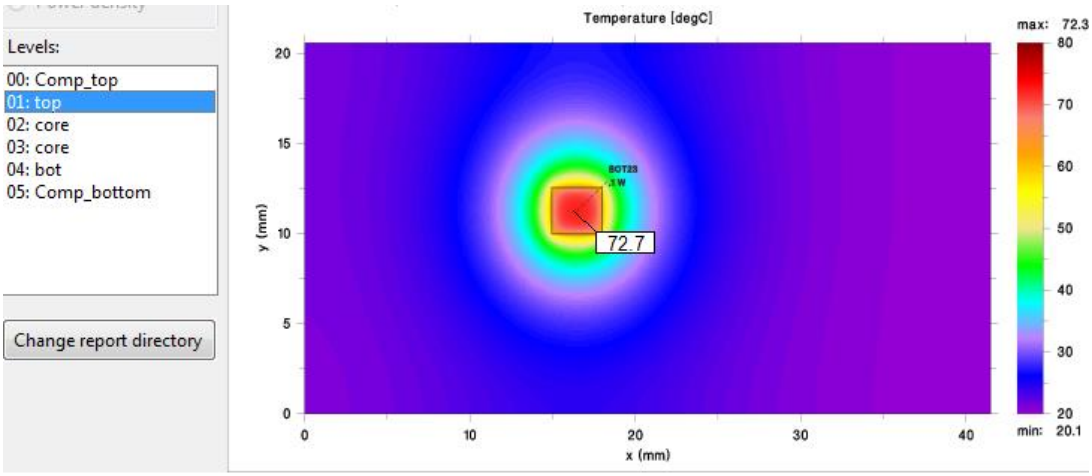

Figure 12: Temperature distribution (halo) in layer 1

and the difference between 77 °C and 72 °C is close to 9 K, which in deed is 90 K/W * 0.1 W – but not perfectly exact that value.

We have to look for two more things: first at the actual heat flux through the bottom face of the component into the board and second at the temperature distribution in layer 1.

First, the heat flux reported at the footprint of SOT23 in `report.txt` is 0.09 W and not 0.1 W:

```
Thermal flux through footprint of top components. + is out, - is in.
    Name                Flux (W)
    SOT23               .091 W
```

If we multiply the thermal resistance with this heat flux, then 90 K/W*0.091 W = 8.2 K which is a bit less than 9 K.

Second, if we observe the variation of temperature in layer 1 underneath the component then we see hotter and colder regions

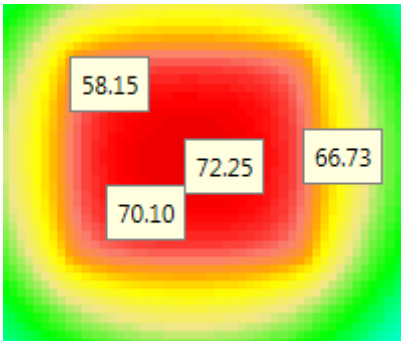

Figure 13: Close-up view of the T-field underneath the component.

For our special board the mean temperature under the component in layer 1 can be extracted using an auxiliary plate of size of SOT21 which has the conductivity of layer 1 but no power

SOT23	15	10	3	2.6	1	0	0	Cu$TRM	r	90	-1	0.1
SOT23_aux	15	10	3	2.6	1	1	1	k=3$TRM	r	-1	-1	0

The answer in file `report.txt` is

```
2 Compon. "SOT23_ 3.000 W/mK  Tmin=  58.057 Tmax=   72.35  Tmean=   68.79 C
```

The mean temperature under the component is 69 °C which is indeed 77 °C - 8 K. This finally shows that the results are consistent and correct within the framework of assumptions and approximations.

The calamity: the calculated junction temperature was 77 °C. What case temperature would that correspond to? From $R_{JA}=R_{JC}+R_{CA}$ we get $R_{CA}=R_{JA}-R_{JC}=239-92 \approx 140$ K/W. Multiplied by 0.1 W: $T_C=20$ °C + 14 K = 34 °C, which is lower than a heated little plate of perfect copper on our test board (=66 °C). The only way to simulate such a cool temperature is to add substantial extra copper in the top layer or to increase the footprint are of the model component.

5 Conclusion

For a good simulation of T_J it is important to have reliable data:

- which test board was used for the data sheet
- what are the correct thermal resistances R_{J-C}, R_{C-B} subject to the cooling conditions in the application
- how large is the heat dissipating foot print area of the component

The published values in data sheets are figures of merit. Precise values should be deliverable by manufacturers on request.

6 Appendix. Survey for more packages

The web site http://www.njr.com/semicon/PDF/package/ae02220.pdf shows values for the J-Ambient and J-Top resistances. J-T is presumably to interpreted at J-C.

The SOT-23 package now has R_{JC} of 70 K/W instead of 90 K/W. This can be due to the layout NJR was using.

Figure 14: „Cu-foil“ applied by NJR in a test board

In general: the larger a component the lower its thermal resistance to ambient. NJR is presenting a parameter study.

■Thermal Resistance of each package

There are typical measured value based on JEDEC with no wind. Each value is dependent on a chip, a layout of a leadframe, a board, and so forth.

Table 3 Thermal resistance of each package

PKG	2 layer board				4 layer board			
	θja (℃/W)	Tj:125℃ Ψjt (℃/W)	Pd (mW)	Tj:150℃ Pd (mW)	θja (℃/W)	Tj:125℃ Ψjt (℃/W)	Pd (mW)	Tj:150℃ Pd (mW)
DMP8	235	47	425	530	175	40	570	710
DMP14	195	47	510	640	150	40	665	830
DMP16	195	47	510	640	150	40	665	830
DMP20	150	37	665	830	120	33	830	1040
SOP8 JEDEC(EMP8)	180	34	555	690	125	29	800	1000
SOP16 JEDEC(EMP16-E2)	110	21	905	1135	70	18	1425	1785
SOP8	165	26	605	755	110	23	905	1135
SOP14	125	21	800	1000	80	17	1250	1560
SOP22	120	18	830	1040	85	14	1175	1470
SOP28	155	37	645	805	125	33	800	1000
SOP40-K1	135	37	740	925	105	33	950	1190
SSOP8	270	42	370	460	210	36	475	595
SSOP8-A3	215	36	465	580	155	15	645	805
SSOP10	270	42	370	460	210	36	475	595
SSOP14	225	38	440	555	180	33	555	690
SSOP16	210	35	475	595	160	26	625	780
SSOP20	185	34	540	675	140	26	710	890
SSOP20-B2	200	34	500	625	150	26	665	830
SSOP20-C3	130	13	765	960	85	9	1175	1470
SSOP32	110	20	905	1135	70	14	1425	1785
SSOP44	110	20	905	1135	70	14	1425	1785
TSSOP54-N1	105	10	950	1190	75	9	1330	1665
HSOP8[4]	160	28	625	780	50	12	2000	2500
HTSSOP24-P1	115	14	865	1085	45	7	2220	2775
MSOP8(TVSP8)	215	27	465	580	160	23	625	780
MSOP10(TVSP10)	215	27	465	580	160	23	625	780
MSOP8(VSP8)	210	33	475	595	155	25	645	805
MSOP10(VSP10)	210	33	475	595	155	25	645	805
SC-82AB	365	89	270	340	255	72	390	490
SC-88A	355	89	280	350	260	73	380	480
SOT-23-5	260	70	380	480	195	60	510	640
SOT-23-6	245	70	405	510	175	60	570	710
SOT-89-3[1][4]	200	67	500	625	130	65	765	960
QFP32-J2	115	17	865	1085	90	15	1110	1385
QFP44-A1	95	17	1050	1315	75	15	1330	1665
QFP48-P1	65	17	1535	1920	50	15	2000	2500
LQFP48-R3	75	9	1330	1665	45	5	2220	2775
LQFP52-H2	85	11	1175	1470	65	11	1535	1920
QFP56-A1	105	17	950	1190	80	15	1250	1560
QFP64-H1	70	17	1425	1785	50	15	2000	2500
LQFP64-H2	65	6	1535	1920	50	5	2000	2500
QFP100-U1	55	5	1815	2270	45	5	2220	2775
TO-252-3[1][4]	105	17	950	1190	40	12	2500	3125
PLCC28	55	10	1815	2270	35	7	2855	3570

PKG	2 layer board				4 layer board			
	Tj:125°C			Tj:150°C	Tj:125°C			Tj:150°C
	θja (°C/W)	Ψjt (°C/W)	Pd (mW)	Pd (mW)	θja (°C/W)	Ψjt (°C/W)	Pd (mW)	Pd (mW)
EPFFP6-A2[2]	370	59	270	335	220	53	450	565
EPFFP10-C4[2]	295	64	335	420	160	55	625	780
PC8P12-C3	240	40	415	520	140	33	710	890
PC8P20-CC	225	40	440	555	140	33	710	890
PC8P20-E3	225	40	440	555	130	33	765	960
PC8P24-ED	205	40	485	605	115	26	865	1085
PC8P32-F7	225	24	440	555	115	17	865	1085
PC8P32-G3[2]	205	24	485	605	115	17	865	1085
PC8P32-GD[2]	205	24	485	605	115	17	865	1085
EPC8P32-L2[2]	210	29	475	595	95	16	1050	1315
DFN6-J1 (SON6-J1)	345	88	285	360	260	69	380	480
DFN4-F1(ESON4-F1)[2]	300	52	330	415	110	27	905	1135
DFN6-H1(ESON6-H1)[2]	280	42	355	445	110	26	905	1135
DFN8-U1(ESON8-U1)[2]	280	43	355	440	110	26	905	1135
DFN8-V1(ESON8-V1)[2]	215	16	465	580	70	8	1425	1785
DFN8-W2(ESON8-W2)[2]	195	21	510	640	60	8	1665	2080
QFN24-T1/T2	150	22	665	830	75	15	1330	1665
EQFN12-E2[2]	285	52	350	435	105	27	950	1190
EQFN12-E4[2]	285	52	350	435	105	27	950	1190
EQFN14-D7[2]	295	53	335	420	95	26	1050	1315
EQFN16-G2[2]	255	43	390	490	100	26	1000	1250
EQFN12-JE[2]	215	22	465	580	80	10	1250	1560
EQFN16-JE[2]	180	21	555	690	70	11	1425	1785
EQFN18-E7[2]	220	33	450	565	90	22	1110	1385
EQFN26-HH[2]	160	15	625	780	60	7	1665	2080
EQFN24-LK[2]	145	13	685	860	65	8	1535	1920

Notes :

1) Thermal resistance values (θ Ja, ψ Jt) are measured with the 2-layer board having 100mm^2 copper foil, which is based on JEDEC.

2) Thermal resistance values (θ Ja, ψ Jt) are measured with the 4-layer board having thermal via holes, which is also based on JEDEC.