How effective are Thermal Vias?

- Less than you think -[1]

Summary

For six assembly layouts, the temperature of the central component is calculated numerically using 3-dimensional circuit board models. The calculation results sometimes with and sometimes without heat vias rarely differ by more than **10%.** Six examples are not proof, but strong evidence.

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[1] Text translated with the help of Google Translate

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Introduction

It is generally believed that copper-plated holes underneath a heating component are helpful for heat dissipation, i.e. cooling. Is it really like that? Is it always like that? After all, there are additional paths for the heat flow from the component to the colder environment

- Direct heat emission from the assembly side to the environment via convection and radiation
- Heat spreading (conduction) within the circuit board into colder areas
- Heat dissipation from the opposite side of the component to the environment

Depending on the layout, number of layers and the arrangement of other heat sources, one or another mechanism can be suppressed and therefore minimized. For example, there is no heat spreading if the assembly is the same temperature everywhere because there are many identical components. On the other hand, heat spreading could be increased by placing a GND layer directly below the main heat source to absorb the heat and transport it away to colder edge areas [1].

Thermal vias are holes that are not necessary for the electronic function, but are intended to carry heat away from the component. I always maintain that thermal vias only make sense if the hole is connected to a heatsink[2]. Then the question arises as to whether you really need extra vias, whether you should fill them, or whether the heat sink alone does a lot of additional cooling work. This will not be examined here.

Someone with many years of experience could possibly be able to preview a design to see whether additional holes (without heat sink) would provide an additional cooling effect. Rth formulas [2] or curves in AppNotes [3] are usually only estimates for the design of a via field because the formulas rarely fit your application or the circuit board used is not representative of your specific heat dissipation task. What cannot be reflected in formulas is the special layout or the so-called heat spreading resistance. Heat always flows away in the prepregs and through the layers of the component anyway. How much heat flow can remain for the vias?

It is not possible to give generally valid recipes; the variety of designs and variants is too great. In this article I choose the empirical route using example calculations based on publicly available evaluation boards from semiconductor manufacturers. But even these assembly designs are in some respects academic and not practical. My tool for the subsequent investigations is numerical calculation of the temperature field using the TRM software from ADAM-Research, which combines layers, layout and drilled holes into a three-dimensional thermal model [4].

I will calculate six designs from the internet, once with vias and once without. If the temperature is roughly the same in both versions, then the vias are ineffective.

Table 1 summarizes the calculation results. The temperature values are given relative to an ambient temperature of 25 °C.

[2] Circuit board, component, vias with heat sinks are the only scenario in which you can get an approximately usable result using a pocket calculator [5].

Table 1. Summary $T\text{-}T_{ambient}$

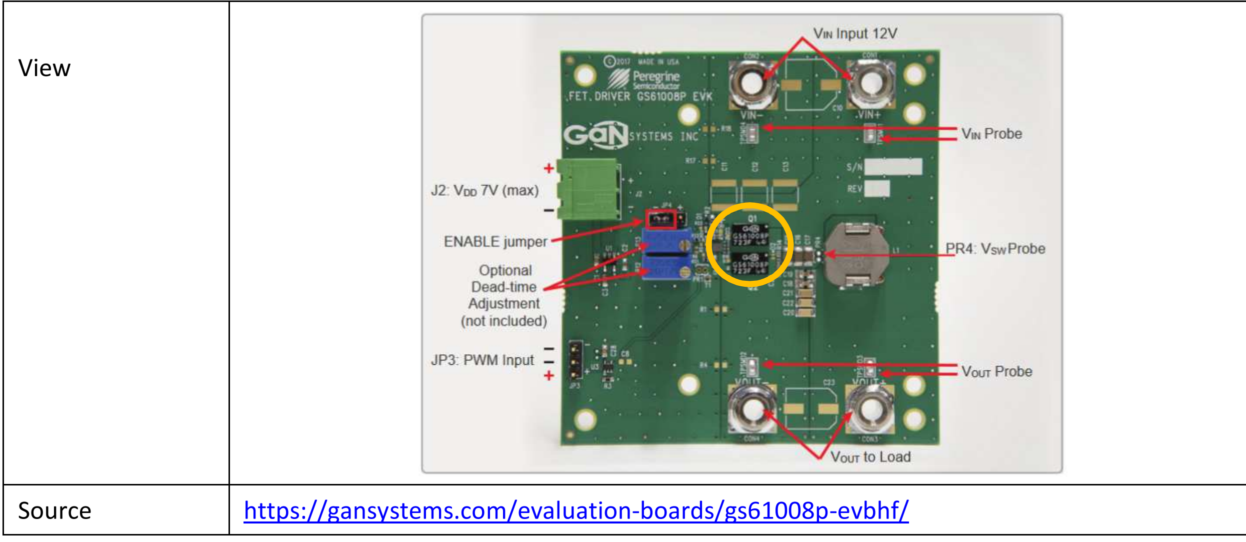
Board Assembly	P_{diss}	With Pad Vias	Without Pad Vias	Comment
GS61008P-EVBHF	2 x 2.5 W	89 K	99 K	Footprint cooling, thermal pad
AEK-AUD-D903V1	5 W	110 K	120 K	Footprint cooling. Slug-down. 20 Vias
		105 K		80 slug vias
		115 K		14 slug vias
DC2387A	7.3 W	85 K	-	BGA signal vias
		80 K	-	plus recommended thermal vias
EVB-USB5806	5 W	95 K	105 K	Footprint slug
MiniPC	30 W	100 K	120 K	BGA vias
ISL8340	8 W	84 K	88 K	Lowest via effecitivty

From Table 1 you can see that there is rarely effective heat dissipation through vias on the evaluation boards. The effect is **around 10%.** Because the final temperature is approximately proportional to the power, the temperature gain due to vias is greater with high power dissipation than with low power. For example, with the second board at 1 W the difference dwindles to 10 K /5 = 2 K.

1. GaNSystems GS61008P-EVBHF

Data

The component is designed to be cooled by the circuit board. Quote from the data sheet: *"The substrate is internally connected to the thermal pad on the bottom-side of the package. The source pad must be electrically connected to the thermal pad for optimal performance. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under this pad will improve thermal performance by reducing the package temperature."*

<table>
<tr><td>View</td><td>
</td></tr>
<tr><td>Source</td><td>https://gansystems.com/evaluation-boards/gs61008p-evbhf/</td></tr>
</table>

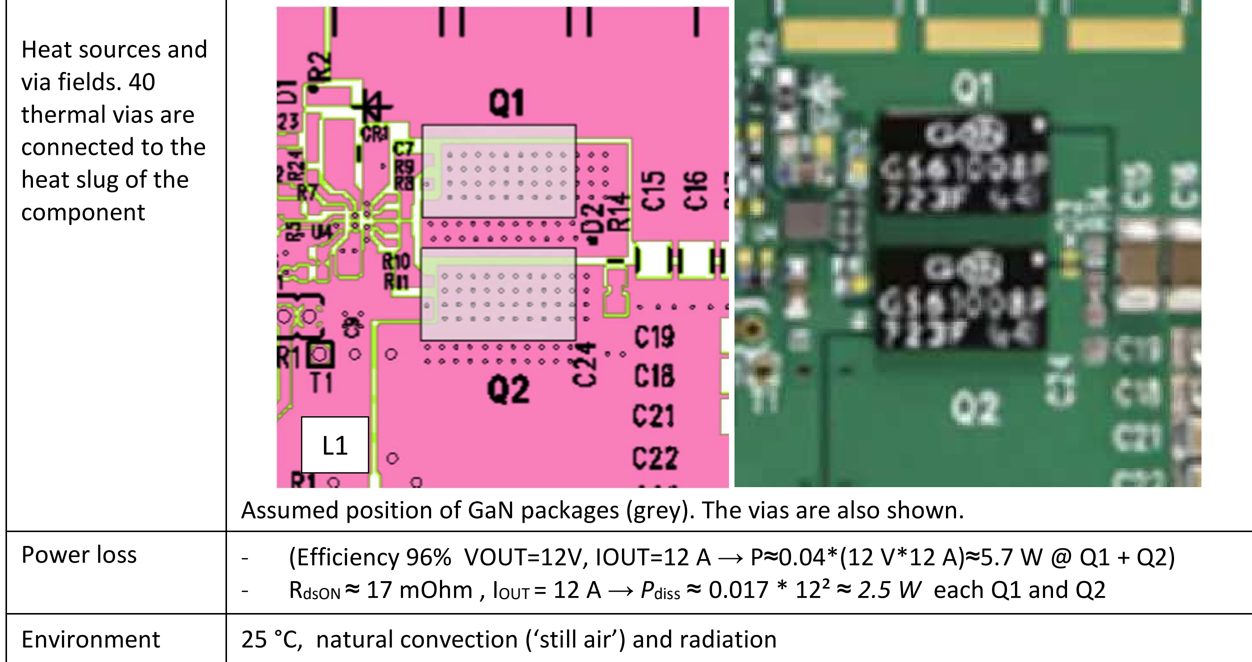
Size	76 mm x 80 mm
Component	Q1, Q2. MOSFET, N-CH, 60V, 50A, TDSON-8 GaN Systems. *Thermal pad*
Data sheet	GS61008P-DS-Rev-200402.pdf Recommended PCB Footprint Package Dimensions - 7.55 mm x 4.6 mm - Drain-to-Source On Resistance $R_{DS(on)}$ 17.5 mΩ @ V_{GS} = 6 V, T_J = 150 °C, I_{DS} = 27 A
Layers	LAYER 1 (TOP SIDE 0.0508mm/.002") FR406 .355mm (.014") CORE LAYER 2 (GND PLANE 0.0508mm/.002) FR406 OR EQUIV. A/R LAYER 3 (GND PLANE 0.0508mm/.002) FR406 .355mm (.014") CORE LAYER 4 (BOTTOM SIDE 0.0508mm/.002) 1.57mm (.062") +/- 10%
Thermal Vias	40 + 40
Experiment	GS61008P-EVBHF-Technical-Manual-Rev-200526.pdf No heat sinking, at room temperature: V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 12A f_{SW} = 1 MHz Figure 10 • GS61008P-EVBHF Evaluation Board (T_{MAX} = 115.3°C) Q1 Q2 GS61008P-EVBHF Rev. 200526 © 2020 GaN Systems Inc. www.gansystems.com Q1≈115 °C, Q2 ≈ 95…100 °C

Model

The data set `RSL10-002GEVB_GERBER.ZIP` only contains Gerber and drill files. There is no placement file included. Therefore, the position of the components is estimated. The power loss value used for the thermal image is also not exactly known and should be between 2.5 W and 2.8 W per Q.

<table>
<tr>
<td>Layer stack

“Silk” is for guidance only</td>
<td>
<table>
<tr><th>Name</th><th>Type</th><th>File</th><th>View</th><th>FR4 white</th><th>Thick (um)</th><th>Conductor</th><th>Dielectric</th><th>Expose</th><th>Color</th></tr>
<tr><td>Silk</td><td>ger</td><td>PRT-69917-01_TS.pho</td><td>View</td><td>✓</td><td>1</td><td>FR4$TRM</td><td>FR4$TRM</td><td>Expose</td><td></td></tr>
<tr><td>L1</td><td>ger</td><td>PRT-69917-01_L1.pho</td><td>View</td><td>✓</td><td>50</td><td>Cu$TRM</td><td>FR4$TRM</td><td>Expose</td><td></td></tr>
<tr><td>pre1</td><td>pre</td><td></td><td>View</td><td>✓</td><td>355</td><td>Cu$TRM</td><td>FR4$TRM</td><td></td><td></td></tr>
<tr><td>L2</td><td>ger</td><td>PRT-69917-01_L2.pho</td><td>View</td><td>✓</td><td>50</td><td>Cu$TRM</td><td>FR4$TRM</td><td>Expose</td><td></td></tr>
<tr><td>pre2</td><td>pre</td><td></td><td>View</td><td>✓</td><td>660</td><td>Cu$TRM</td><td>FR4$TRM</td><td></td><td></td></tr>
<tr><td>L3</td><td>ger</td><td>PRT-69917-01_L3.pho</td><td>View</td><td>✓</td><td>50</td><td>Cu$TRM</td><td>FR4$TRM</td><td>Expose</td><td></td></tr>
<tr><td>pre3</td><td>pre</td><td></td><td>View</td><td>✓</td><td>355</td><td>Cu$TRM</td><td>FR4$TRM</td><td></td><td></td></tr>
<tr><td>L4</td><td>ger</td><td>PRT-69917-01_L4.pho</td><td>View</td><td>✓</td><td>50</td><td>Cu$TRM</td><td>FR4$TRM</td><td>Expose</td><td></td></tr>
</table>
</td>
</tr>
<tr>
<td>Layers 1 to 4 with 10x4 PTH Vias under each component</td>
<td>The conditions for Q1 and Q2 are not identical.</td>
</tr>
</table>

Heat sources and via fields. 40 thermal vias are connected to the heat slug of the component	 Assumed position of GaN packages (grey). The vias are also shown.
Power loss	- (Efficiency 96% VOUT=12V, IOUT=12 A ⟶ P≈0.04*(12 V*12 A)≈5.7 W @ Q1 + Q2) - R_{dsON} ≈ 17 mOhm , I_{OUT} = 12 A ⟶ P_{diss} ≈ 0.017 * 12^2 ≈ *2.5 W* each Q1 and Q2
Environment	25 °C, natural convection ('still air') and radiation

Calculation Results

The model contains approx. 4.2 million temperature nodes with a horizontal resolution of 0.1 mm. The calculation takes only a few seconds. The results for all layers and prepregs are available as pictures and tables.

Q1 and Q2 have different cooling conditions. Q1 is firstly located in a narrowed copper geometry in L1 (horizontal color edge with a sharp transition from yellow to light blue between VIN and RETURN) and secondly above copper holes = FR4 islands in L2, L3 and L4. The reason for the copper holes is unknown to us. Hence Q1 is warmer than Q2. The difference in temperature can also be seen in the other layers immediately below Q1 and Q2.

Experience from other previous projects shows that the calculated component temperatures with the thermal camera within proximately 5% if the power loss is given correctly. Additional uncertainties include the thermal conductivity of the prepregs, the actual thicknesses of layers and prepregs and the internal structure of the components.

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With Pad Vias

Temperature L1 Semitransparent components and drilled holes Q1=2.5 W Q2=2.5 W Ambient temper-ature 25 °C	
Temperature L1 and L4 116°C , 113°C (Vias are not drawn)	

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WithoutThermal Pad Vias

L1 , L4 tempera-ture

124 °C , 109 °C

Without Thermal Pad Vias

L1 in two repre-sentations

In this design, the pad vias have a moderate influence on temperature. This can be seen in the temperature of L1. For Q1 the gain from the thermal vias corresponds to approx. 99 K/89 K ≈ 10%. Q2 has a better ratio because there are no copper voids in the inner layers underneath.

Table 2. Relative max. temperature above ambient in L1

GS61008P-EVBHF	Q1 ΔT (K)	Q2 ΔT (K)
Experiment	≈ 90	≈75
TRM with Pad Vias	≈ 89	≈ 80
TRM without Pad Vias	≈ 99	≈ 90

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2. STMicroelectronics AEK-AUD-D903V1

Quote from the data sheet “*This system is required by new vehicles to alert pedestrians of the presence of electric powered vehicles that are generating much less noise. Warning sounds may be driver triggered (like a horn) or automatic mimicking engine sounds. From 2021 according to government regulations, the vehicle must make a continuous noise level of at least 56 dBA (within 2 meters) if the car is going 20 km/h (12 mph) or slower, and a maximum of 75 dBA. The FDA903D amplifier comes in a PowerSSO-36 slug-down package and features a configurable power limiting function, high-speed I²C and legacy mode interfaces, and an internal finite state machine*.”

Data

View	**Features** • With FDA903D class D automotive grade audio amp • Mono channel up to 45 W • Supports audio stream via I²S interface • Configurable through dedicated I²C bus • Dedicated DC diagnostic interrupt pin to signal faults • Dedicated hardware MUTE pin
Source	https://www.st.com/en/evaluation-tools/aek-aud-d903v1.html https://www.st.com/resource/en/data_brief/aek-aud-d903v1.pdf
Size	79 mm x 52 mm
Component	U1 FDA903D-EHT PSSO-36 1/10W ±5% 1 x 45 W class D digital input automotive power amplifier
Data sheet	https://www.st.com/en/automotive-infotainment-and-telematics/fda903d.html https://www.st.com/resource/en/datasheet/fda903d.pdf Slug - down - 7.5 mm x 10.3 mm
Layers	Not specified Assumption: https://www.st.com/resource/en/application_note/an5407-how-to-optimize-the-rf-board-layout-for-stm32wl5xex-mcus-stmicroelectronics.pdf

	• **Case 3**: typical stack-up for BGA package with **PCB total thickness = 1.60 mm** Consider the configuration detailed in the table below.
Thermal Vias	20
Experiments	Table 4. Thermal data - PowerSSO36 slug-down package

Table 15. **Case 3: PCB total thickness = 1.60 mm**

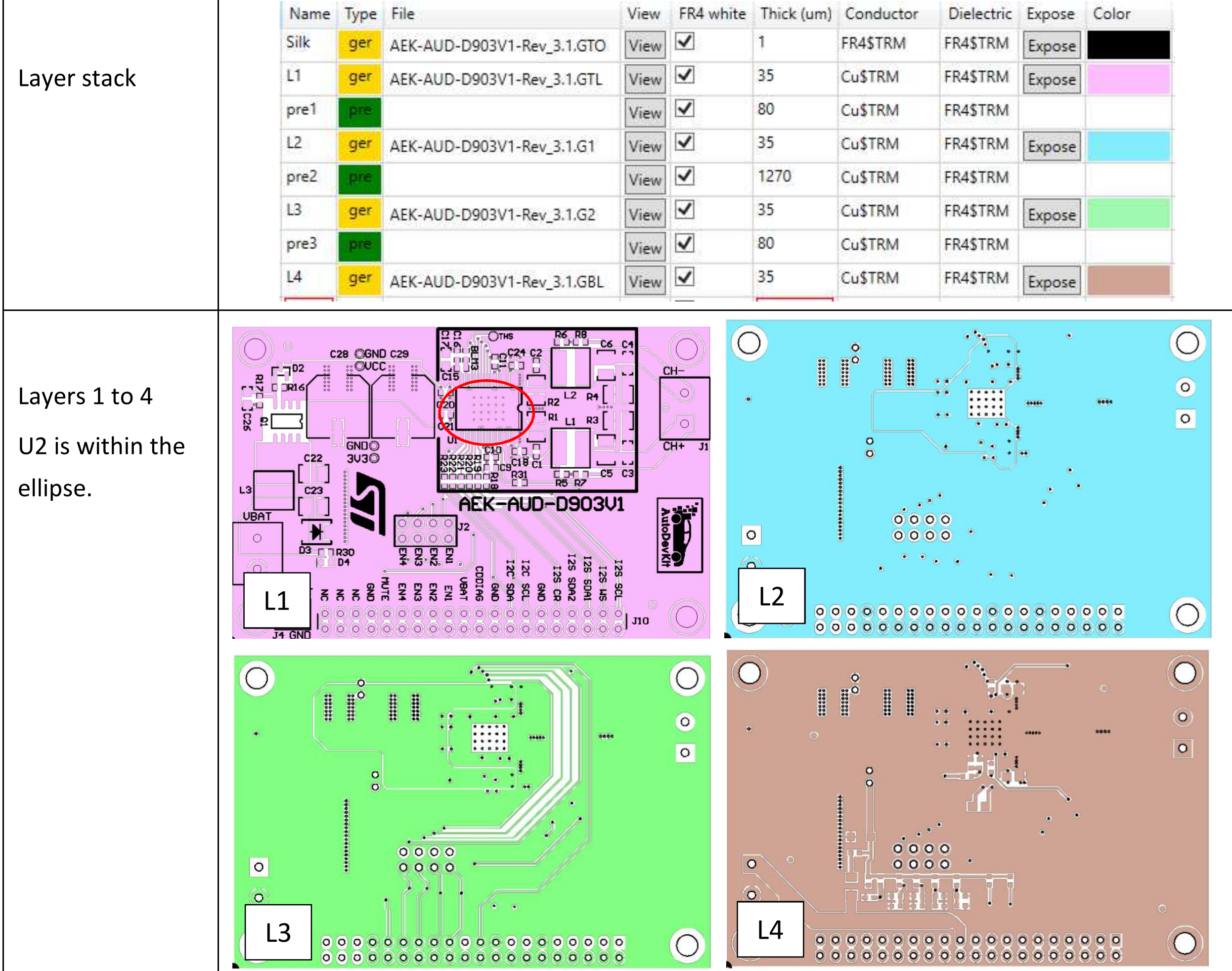
Dielectric materials				Metal layers	
Element	Material	Nominal thickness h_x (µm)	ε_r	Layer	Nominal thickness t (µm)
Solder mask (h_3)	solder resist	20	3.5	Top	35
Prepreg 1 (h_1)	1 x 1080	76	4.18	Middle 1 and 2	35
Core (h_2)	7 x 7628	1268	4.74	Bottom	35

Table 4. Thermal data - PowerSSO36 slug-down package

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}a\text{-}2s}$	Thermal resistance junction-to-ambient (2s board)	56	°C/W
$R_{th\ j\text{-}a\text{-}2s2p}$	Thermal resistance junction-to-ambient (2s2p board)	31	°C/W
$R_{th\ j\text{-}a\text{-}2s2pv}$	Thermal resistance junction-to-ambient (2s2p+vias)	26	°C/W

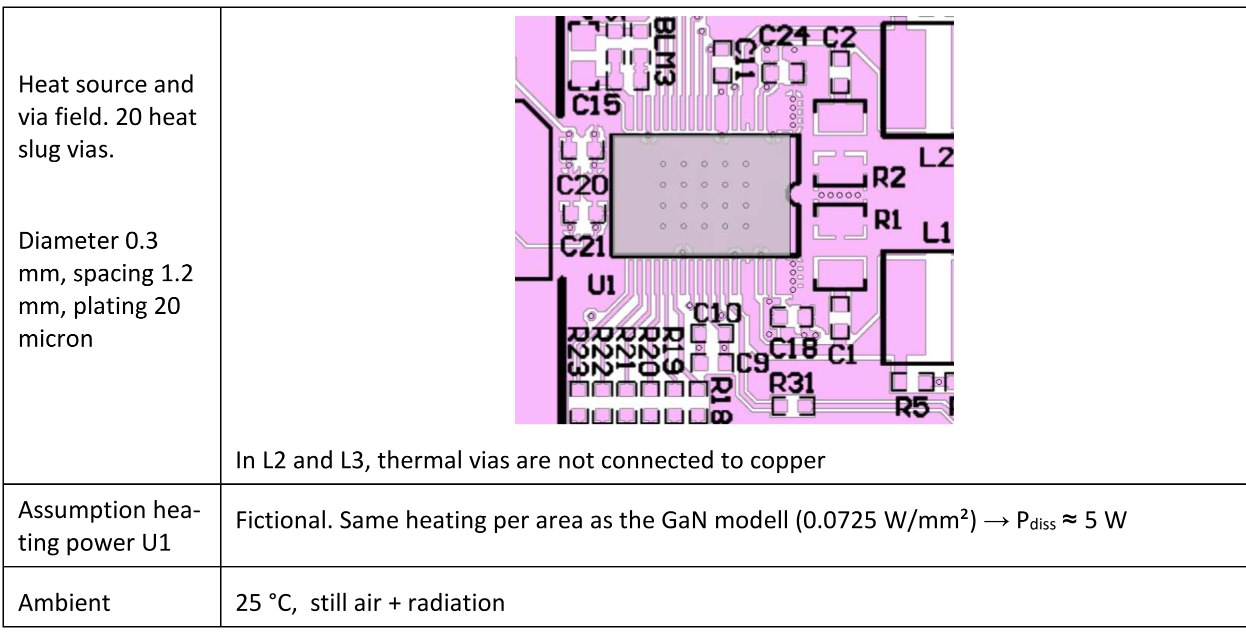
Model

The data set `aek-aud-d903v1_gerber.zip` contains Gerber- and drill files only (https://www.st.com/resource/en/board_manufacturing_specification/aek-aud-d903v1_gerber.zip). I set the power loss for the calculation to 5 W.



Layer stack

Name	Type	File	View	FR4 white	Thick (um)	Conductor	Dielectric	Expose	Color
Silk	ger	AEK-AUD-D903V1-Rev_3.1.GTO	View	☑	1	FR4$TRM	FR4$TRM	Expose	
L1	ger	AEK-AUD-D903V1-Rev_3.1.GTL	View	☑	35	Cu$TRM	FR4$TRM	Expose	
pre1	pre		View	☑	80	Cu$TRM	FR4$TRM		
L2	ger	AEK-AUD-D903V1-Rev_3.1.G1	View	☑	35	Cu$TRM	FR4$TRM	Expose	
pre2	pre		View	☑	1270	Cu$TRM	FR4$TRM		
L3	ger	AEK-AUD-D903V1-Rev_3.1.G2	View	☑	35	Cu$TRM	FR4$TRM	Expose	
pre3	pre		View	☑	80	Cu$TRM	FR4$TRM		
L4	ger	AEK-AUD-D903V1-Rev_3.1.GBL	View	☑	35	Cu$TRM	FR4$TRM	Expose	

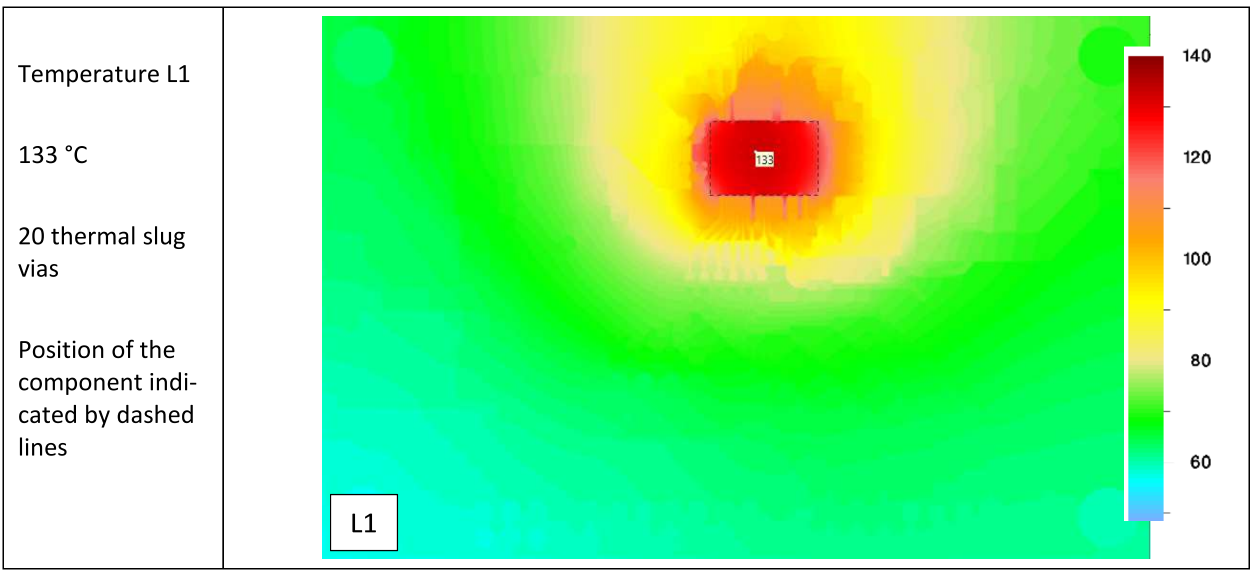


Heat source and via field. 20 heat slug vias. Diameter 0.3 mm, spacing 1.2 mm, plating 20 micron	In L2 and L3, thermal vias are not connected to copper
Assumption heating power U1	Fictional. Same heating per area as the GaN modell (0.0725 W/mm²) ⟶ P_{diss} ≈ 5 W
Ambient	25 °C, still air + radiation

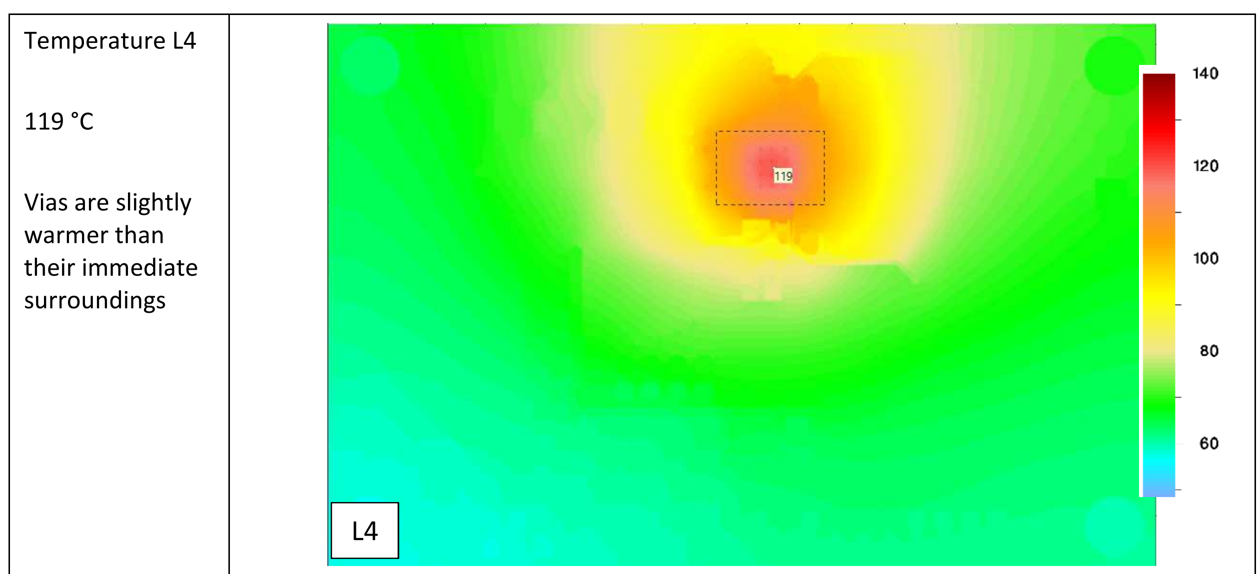
Calculation results

The model contains approximately 2.9 million temperature nodes at a horizontal resolution of 0.1 mm. U1 is hotter than in the GaN model for the same power per mm². The extent to which the prepregs' thicknesses have influence should not be examined here.

With 20 heat slug vias

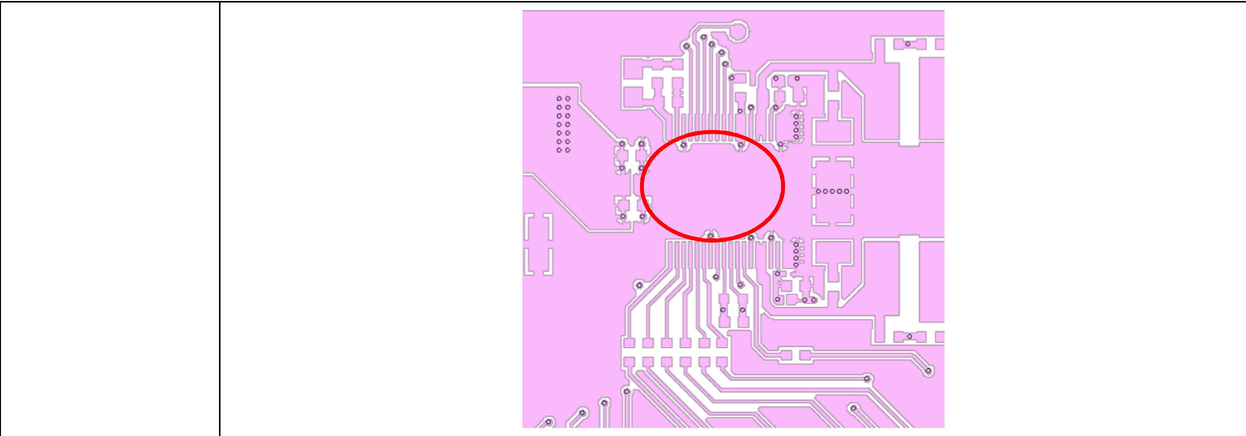


Temperature L1 133 °C 20 thermal slug vias Position of the component indicated by dashed lines	

Temperature L4 119 °C Vias are slightly warmer than their immediate surroundings	

The mean component temperature is about. 133 °C. This results in $R_{\theta\ \text{surf-ambient}} \approx (133-25)\ \text{K}/5\ \text{W} \approx 20\ \text{K/W}$.

Without heat slug vias

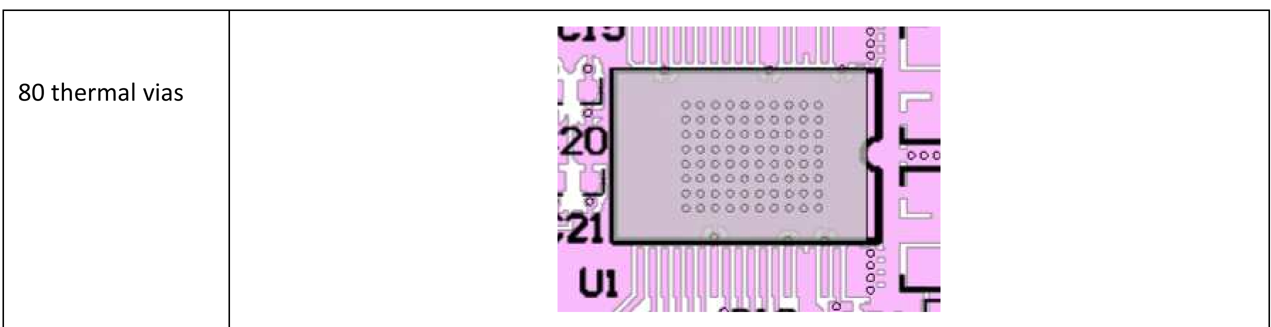
	

Temperature L1 143 °C Component transparent	
Temperatur L4 105 °C	

The through-plane temperature difference at 40 K is much steeper without vias. The top layer gets hotter, the bottom layer gets colder because the temperature equalization by vias is missing.

With 80 heat slug vias

I increase the number of vias from 20 to 80 while maintaining the same diameters and plating. Distance now 0.6 mm.

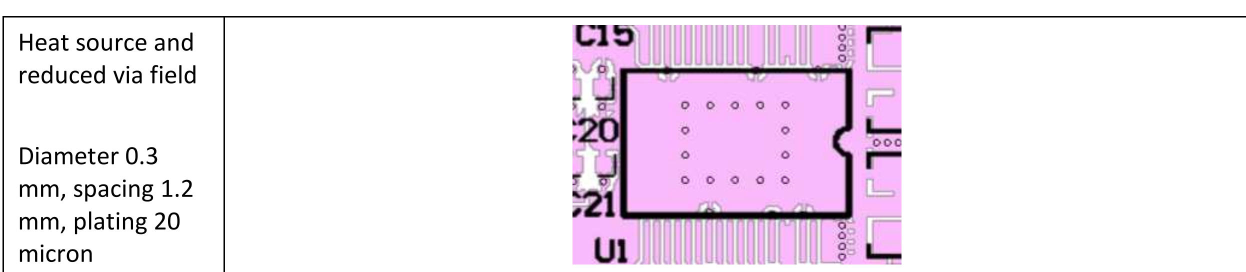
80 thermal vias	

Temperature L1 130 °C Marginal im-provement by -2K	
Temperature L4 126 °C Layer 4 is getting warmer in the center with 80 vias but the mean value hardly changes.	

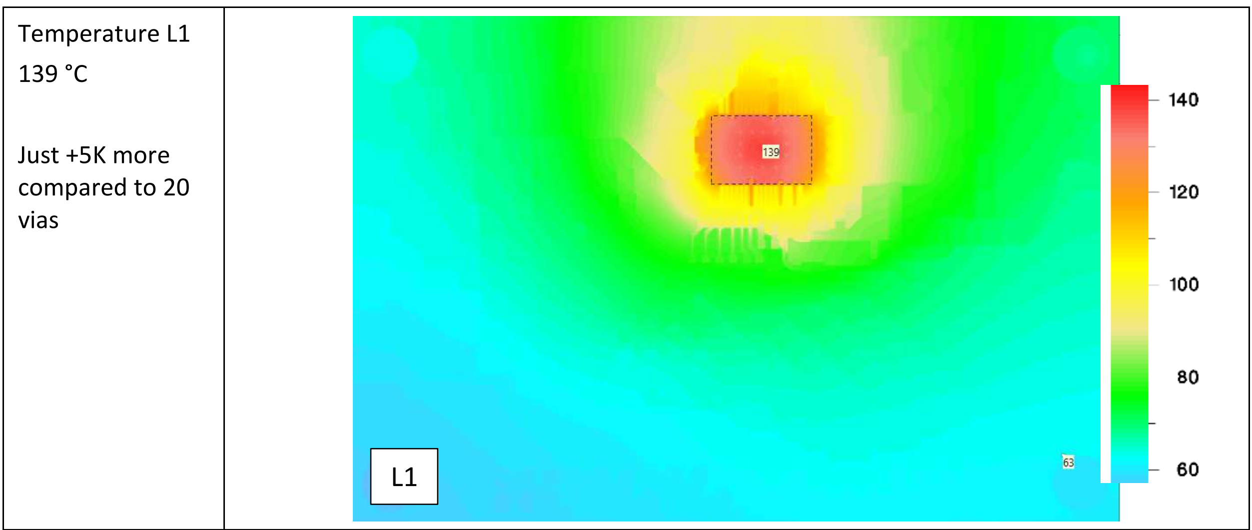
The more vias, the greater the vertical effective thermal conductivity of the vias area. If the vias ended on a good heatsink, that would result in better (but not necessarily proportional) cooling. In this case, the heat absorptive capacity of the top and bottom layers appears to be exhausted. Heat spreading on top layer is geometrically interrupted by the fiberized conductor tracks and the insulations between.

With 14 heat slug vias

Inside the original via field, the temperature (in steady state) is roughly evenly distributed. Where there is no temperature difference, no heat can flow. Let's check whether just the edge vias might be sufficient.



Heat source and reduced via field Diameter 0.3 mm, spacing 1.2 mm, plating 20 micron	

Temperature L1 139 °C Just +5K more compared to 20 vias	

3. Analog DC2387A

To what extent do vias under a BGA contribute to cooling and what are the benefits of additional thermal vias?

Quoting from documentation: “*Demonstration circuit 2387A features the LTM®8071 µModule® regulator, a high performance, high efficiency Silent Switcher® step-down regulator. The LTM8071 is a complete DC/DC point-of-load regulator in* *a thermally enhanced* *11.25mm × 9mm × 3.32mm BGA package*.”

Data

View	
Source	https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/dc2387a.html#eb-documentation
Size	76 mm x 76 mm
Component	https://www.analog.com/media/en/technical-documentation/data-sheets/ltm8071.pdf 11.25mm × 9mm × 3.32mm BGA package

	BGA PACKAGE 80-LEAD (11.25mm × 9mm × 3.32mm) T_{JMAX} = 125°C, θ_{JA} = 18°C/W, $\theta_{JCbottom}$ = 3.4°C/W, θ_{JCtop} = 8.4°C/W, θ_{JB} = 2.8°C/W, WEIGHT = 1.0g θ VALUES DETERMINED PER JESD 51-9, 51-12
Layer stack	LAYER STRUCTURE
Experiment P_{diss} not known	DC2387A.pdf https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/dc2387a.html#eb-documentation No heat sinking, at room temperature Figure 6. Measured Thermal Capture at $48V_{IN}$, $5A_{OUT}$ at 25°C Ambient with No Airflow

Model

Gerber and drill files can be found at: https://www.analog.com/media/en/evaluation-documentation/evaluation-design-files/DC2387A.zip. The proposed 25 additional thermal vias are not included in the .zip file.

<table>
<tr><td>Layer stack</td><td>
<table>
<tr><th>Level</th><th>Name</th><th>Type</th><th>File</th><th>View</th><th>FR4 white</th><th>Thick (um)</th><th>Conductor</th><th>Dielectric</th><th>Expose</th><th>Color</th></tr>
<tr><td>1</td><td>Silk</td><td>ger</td><td>TS.pho</td><td>View</td><td>☑</td><td>1</td><td>FR4$TRM</td><td>FR4$TRM</td><td>Expose</td><td></td></tr>
<tr><td>2</td><td>L1</td><td>ger</td><td>L1.pho</td><td>View</td><td>☑</td><td>70</td><td>Cu$TRM</td><td>FR4$TRM</td><td>Expose</td><td></td></tr>
<tr><td>3</td><td>pre1</td><td>pre</td><td></td><td>View</td><td>☑</td><td>90</td><td>Cu$TRM</td><td>FR4$TRM</td><td></td><td></td></tr>
<tr><td>4</td><td>L2</td><td>ger</td><td>L2.pho</td><td>View</td><td>☑</td><td>35</td><td>Cu$TRM</td><td>FR4$TRM</td><td>Expose</td><td></td></tr>
<tr><td>5</td><td>core</td><td>pre</td><td></td><td>View</td><td>☑</td><td>1210</td><td>Cu$TRM</td><td>FR4$TRM</td><td></td><td></td></tr>
<tr><td>6</td><td>L3</td><td>ger</td><td>L3.pho</td><td>View</td><td>☑</td><td>35</td><td>Cu$TRM</td><td>FR4$TRM</td><td>Expose</td><td></td></tr>
<tr><td>7</td><td>pre3</td><td>pre</td><td></td><td>View</td><td>☑</td><td>90</td><td>Cu$TRM</td><td>FR4$TRM</td><td></td><td></td></tr>
<tr><td>8</td><td>L4</td><td>ger</td><td>L4.pho</td><td>View</td><td>☑</td><td>70</td><td>Cu$TRM</td><td>FR4$TRM</td><td>Expose</td><td></td></tr>
</table>
</td></tr>
<tr><td>Layers 1 to 4</td><td>L1
L2
L3
L4</td></tr>
<tr><td>Heat source and via field

Vias are con-nected to copper in all layers

Diameter0.125 mm, spacing 1.0 mm, plating 20 micron</td><td></td></tr>
<tr><td>Assumed heating power U1</td><td>Fictional. Same heat per area as in GaN model (0.0725 W/mm²) ⟶ P_{diss} ≈ 7.3 W (!)</td></tr>
<tr><td>Ambient</td><td>25 °C, still air + radiation</td></tr>
</table>

Calculation results

The model contains approximately 4.6 million temperature nodes at a horizontal resolution of 0.1 mm. Because there are few interruptions in the layers, the heat spread works very well.

Original vias

Temperature L1 Original via field 110 °C	
Temperature L4 92 °C	

With thermal vias

The extra thermal vias shown in the data sheet are not included in the drill file and are added manually. Diameter 0.254 mm, like the majority of the other holes.

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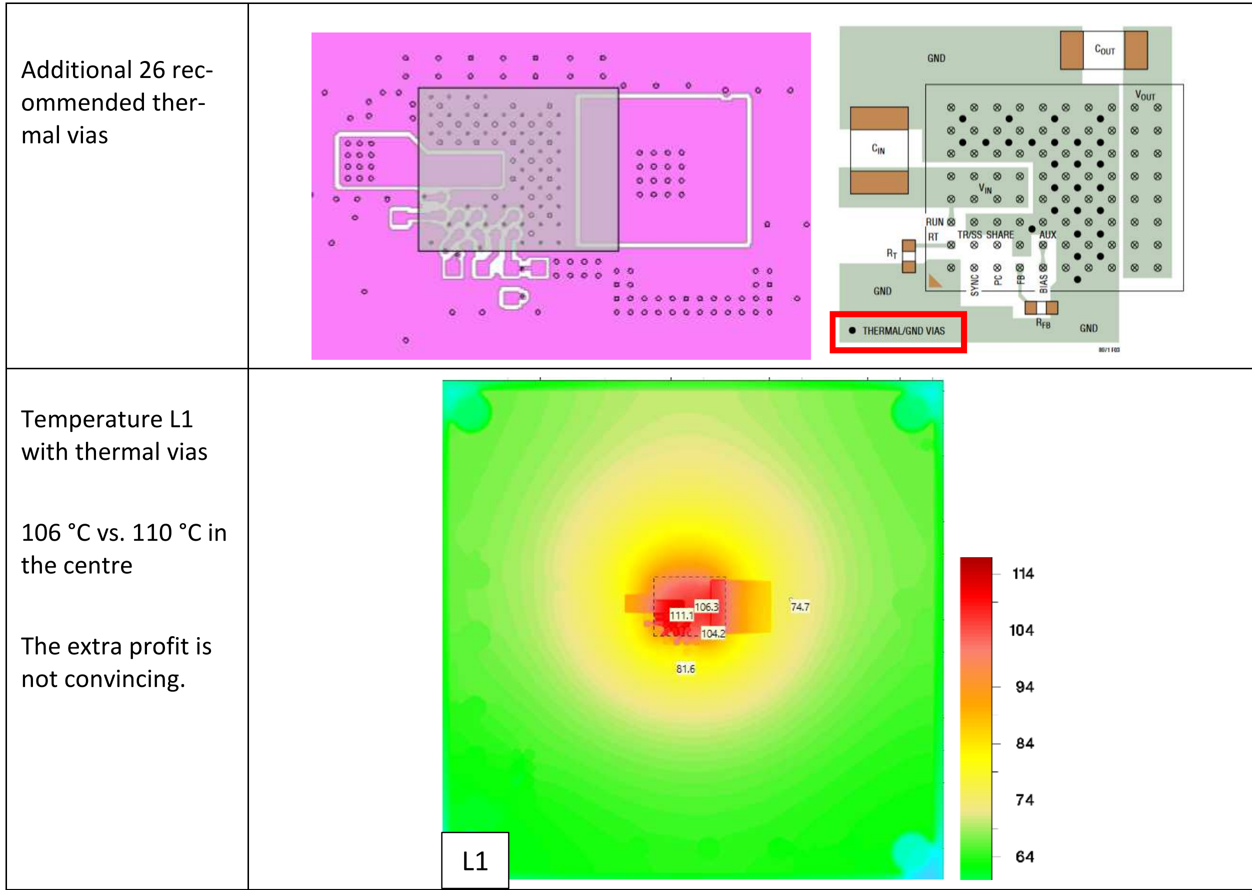


Additional 26 recommended thermal vias	
Temperature L1 with thermal vias 106 °C vs. 110 °C in the centre The extra profit is not convincing.	

4. Microchip EVB-USB5806

The evaluation boards examined so far have been characterized by generous heat spreading. Although high heat losses are not to be expected with this board, the shape of the signals under and around U1 is interesting enough to investigate.

Data

View	USB5806 USB3.2 GEN1 6-P • Microchip’s FlexConnect, PortSwap, PHYBoost™, and VariSense™ technologies • USB5806 in a 100-pin QFN RoHS compliant package • USB 3.2 Gen 1 compliant (SS, HS, FS, and LS operation) • USB pins are 5 V tolerant • Self powered operation • Six downstream USB 2.0 / USB 3.2 Gen 1 ports
Source	https://www.microchip.com/en-us/development-tool/evb-usb5806
Size	127 mm x 76 mm
Component	U1 IC, USB58xx, USB59xx, 7 Port USB 3.1 Gen1 Hub, QFN100 Microchip Technology

Layer stack	
Thermal Vias	36

Layer stack:

Name	Material	Type	Weight	Thickness
Top Overlay		Overlay		
Top Solder	Solder Resist	Solder Mask		0.4mil
Top Layer 1		Signal	1oz	2mil
Dielectric1	370HR(1ply 1...	Prepreg		4.3mil
Inner Layer 2		Plane	1oz	1.4mil
Dielectric 2	370HR	Core		47mil
Inner Layer 3		Plane	1oz	1.4mil
Dielectric 3	370HR(1ply 1...	Prepreg		4.3mil
Bottom Layer 4		Signal	1oz	2mil

Model

Gerber and Altium files are available. Altium designs can be imported with TRM almost automatically.
https://ww1.microchip.com/downloads/en/DeviceDoc/EVB-USB580x_A-AltiumFiles.zip

Layer stack:

Name	Type	File	View	FR4 white	Thick (um)	Conductor	Dielectric	Expose	Color
Silk	ger	EVB-USB580x.GTO	View	☑	1	Cu$TRM	FR4$TRM	Expose	
Top Layer	ger	EVB-USB580x.GTL	View	☑	51	Cu$TRM	FR4$TRM	Expose	
Dielectric	pre		View	☑	109	Cu$TRM	FR4$TRM		
Internal Plane 1	ger	EVB-USB580x.GP1	View	☐	36	Cu$TRM	FR4$TRM	Expose	
Dielectric	pre		View	☑	1194	Cu$TRM	FR4$TRM		
Internal Plane 2	ger	EVB-USB580x.GP2	View	☐	36	Cu$TRM	FR4$TRM	Expose	
Dielectric	pre		View	☑	109	Cu$TRM	FR4$TRM		
Bottom Layer	ger	EVB-USB580x.GBL	View	☑	51	Cu$TRM	FR4$TRM	Expose	

Layers 1 to 4:

L1 L2 L3 L4

Heat source U1 and original vias
Diameter 0.25 mm, distance 1.2 mm, plating 20 micron:

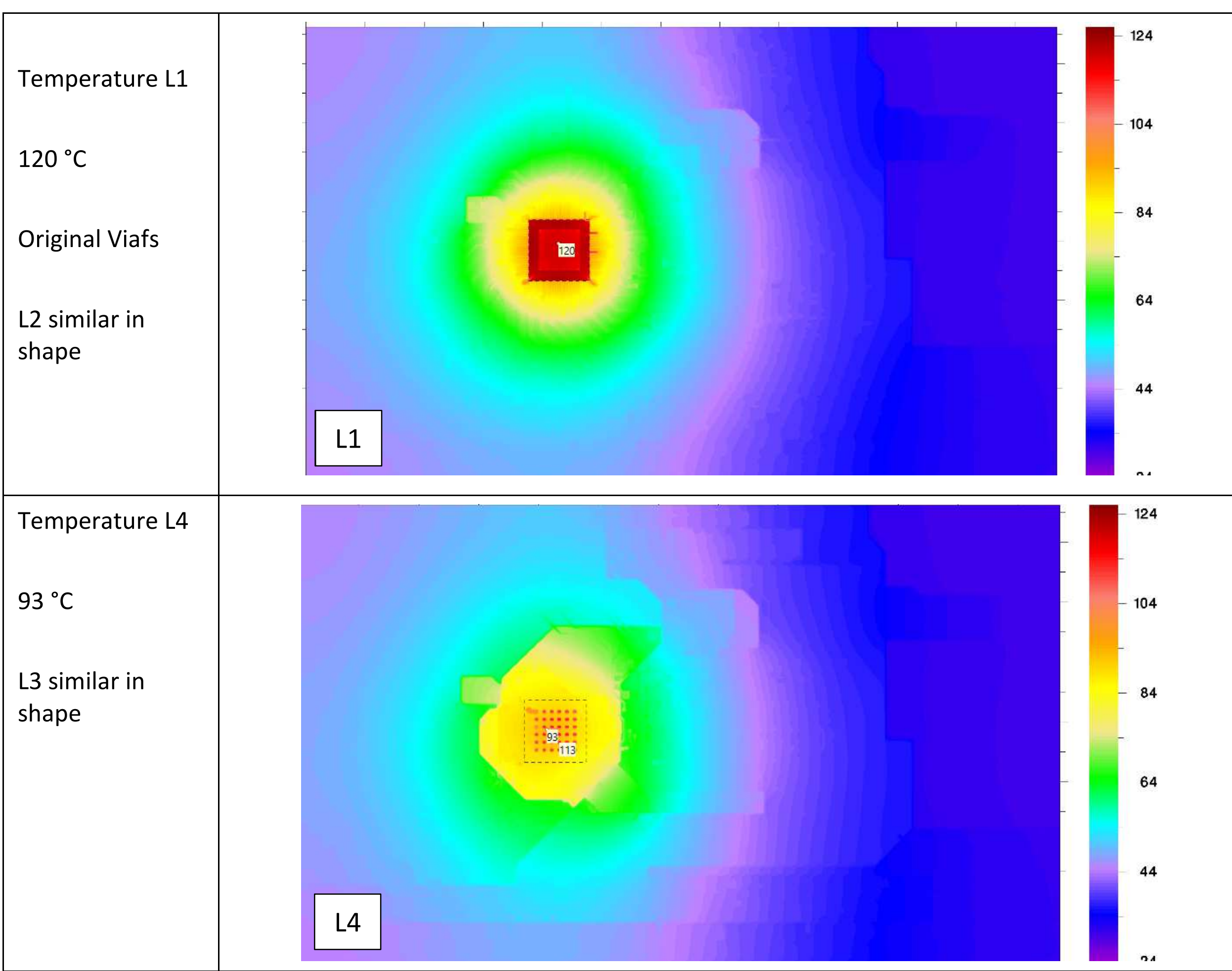
Vias are contaced to copper in L1 and L2 only

Assumed heating power	Fictitious. 5 W to be comparable with the other models.
Ambient	25 °C, still air + radiation

Calculation results

The model contains approximately 7.7 million temperature nodes at a horizontal resolution of 0.1 mm.

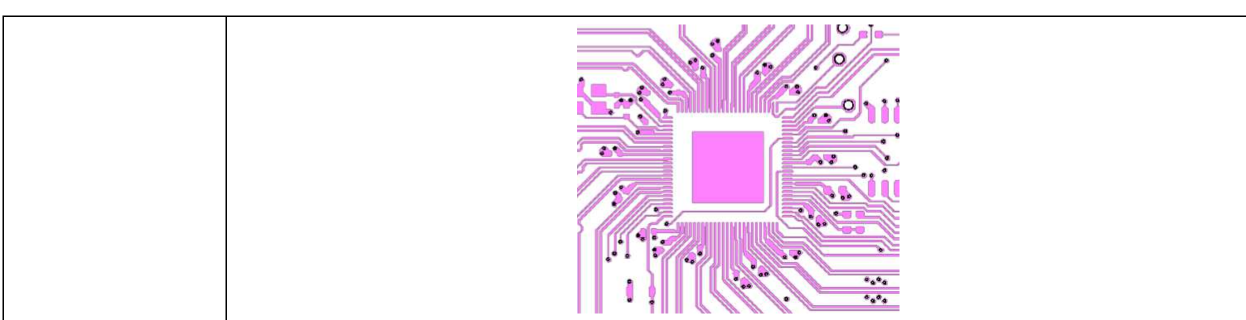
Original heat slug vias

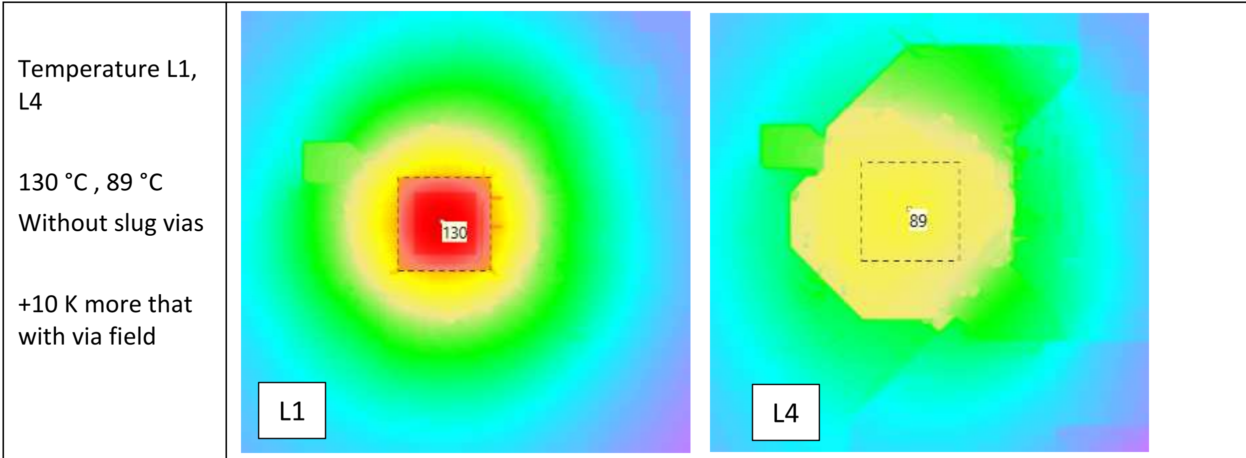


Temperature L1 120 °C Original Viafs L2 similar in shape	
Temperature L4 93 °C L3 similar in shape	

The vias on L4 are hot (113°C) because the heat fed into them by the component cannot easily escape from the anti-pads.

Without heat slug vias

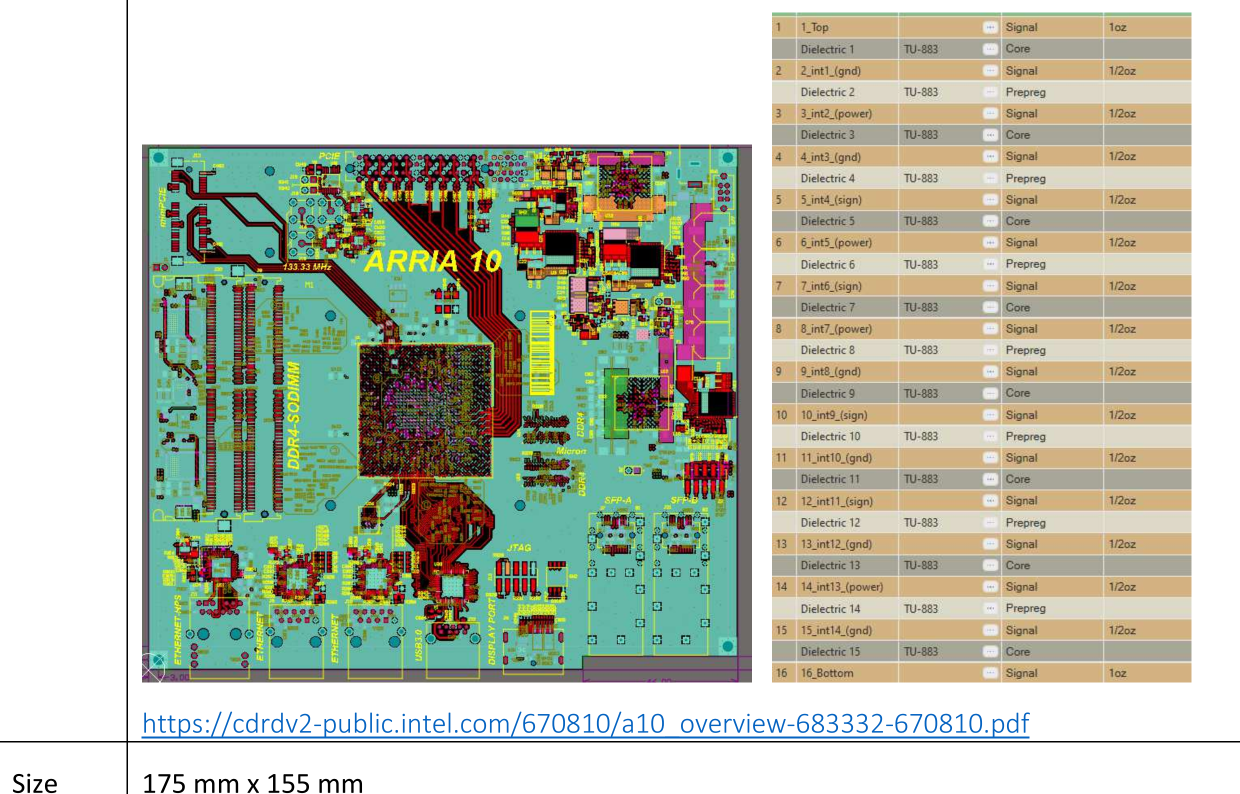


Temperature L1, L4 130 °C , 89 °C Without slug vias +10 K more that with via field	

5. MiniPC

The "MiniPC" is part of the demo boards of an Altium Designer® installation. What makes the board interesting are its 16 layers (!) and the large BGA with its many vias (through-holes and back-drills). It is sometimes claimed that the heat dissipation of such components should work well due to the many connections alone. The original design actually contains a matching BGA fan, which we of course don't take into account here.

Data



1	1_Top		Signal	1oz
	Dielectric 1	TU-883	Core	
2	2_int1_(gnd)		Signal	1/2oz
	Dielectric 2	TU-883	Prepreg	
3	3_int2_(power)		Signal	1/2oz
	Dielectric 3	TU-883	Core	
4	4_int3_(gnd)		Signal	1/2oz
	Dielectric 4	TU-883	Prepreg	
5	5_int4_(sign)		Signal	1/2oz
	Dielectric 5	TU-883	Core	
6	6_int5_(power)		Signal	1/2oz
	Dielectric 6	TU-883	Prepreg	
7	7_int6_(sign)		Signal	1/2oz
	Dielectric 7	TU-883	Core	
8	8_int7_(power)		Signal	1/2oz
	Dielectric 8	TU-883	Prepreg	
9	9_int8_(gnd)		Signal	1/2oz
	Dielectric 9	TU-883	Core	
10	10_int9_(sign)		Signal	1/2oz
	Dielectric 10	TU-883	Prepreg	
11	11_int10_(gnd)		Signal	1/2oz
	Dielectric 11	TU-883	Core	
12	12_int11_(sign)		Signal	1/2oz
	Dielectric 12	TU-883	Prepreg	
13	13_int12_(gnd)		Signal	1/2oz
	Dielectric 13	TU-883	Core	
14	14_int13_(power)		Signal	1/2oz
	Dielectric 14	TU-883	Prepreg	
15	15_int14_(gnd)		Signal	1/2oz
	Dielectric 15	TU-883	Core	
16	16_Bottom		Signal	1oz

https://cdrdv2-public.intel.com/670810/a10_overview-683332-670810.pdf

Size	175 mm x 155 mm

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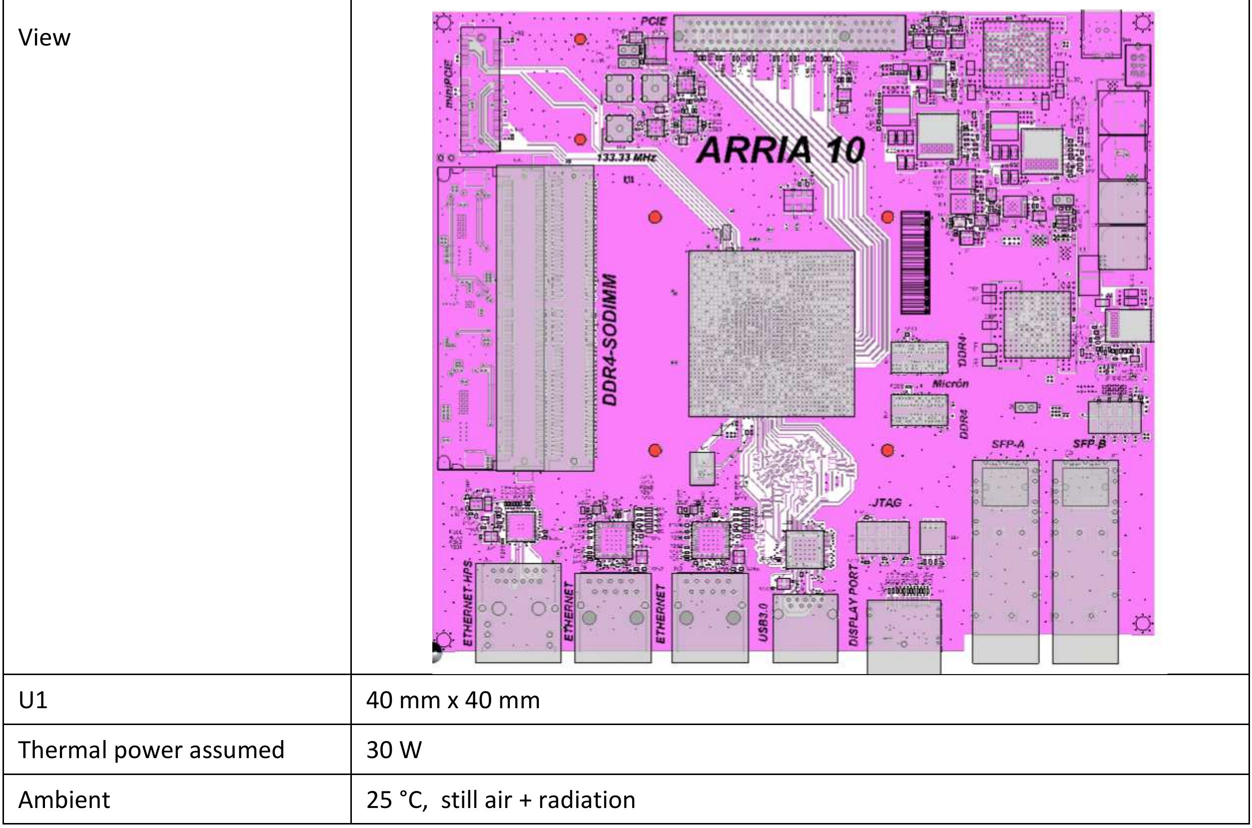
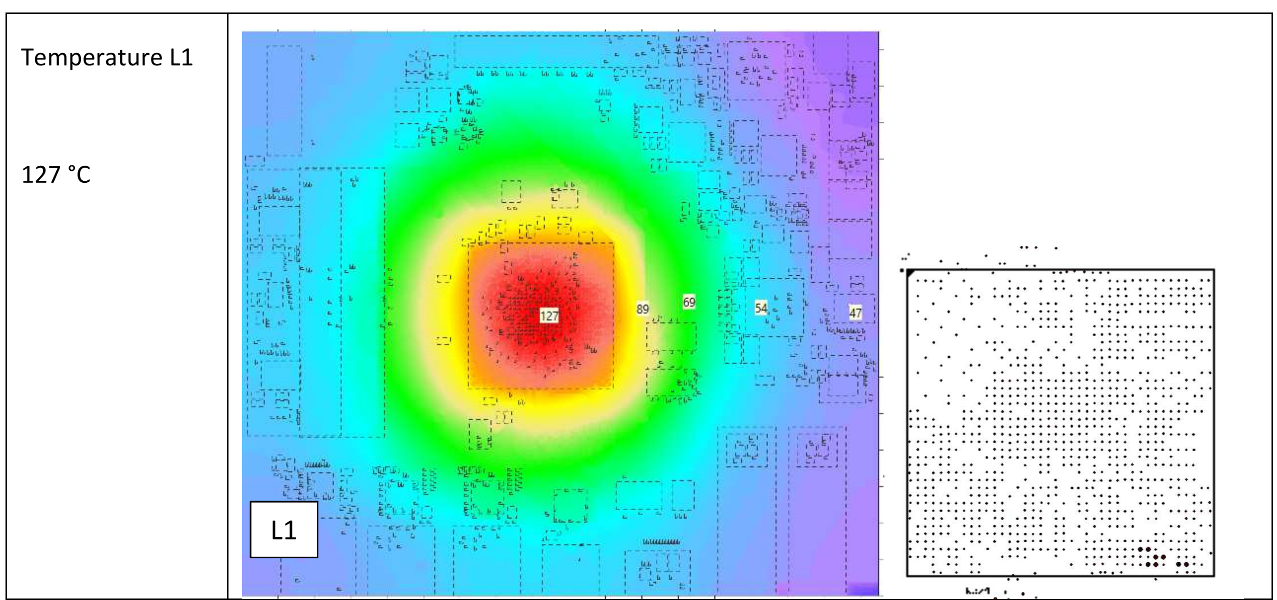
Model

View	
U1	40 mm x 40 mm
Thermal power assumed	30 W
Ambient	25 °C, still air + radiation

Calculation results

Original BGA vias

Temperature L1 127 °C	

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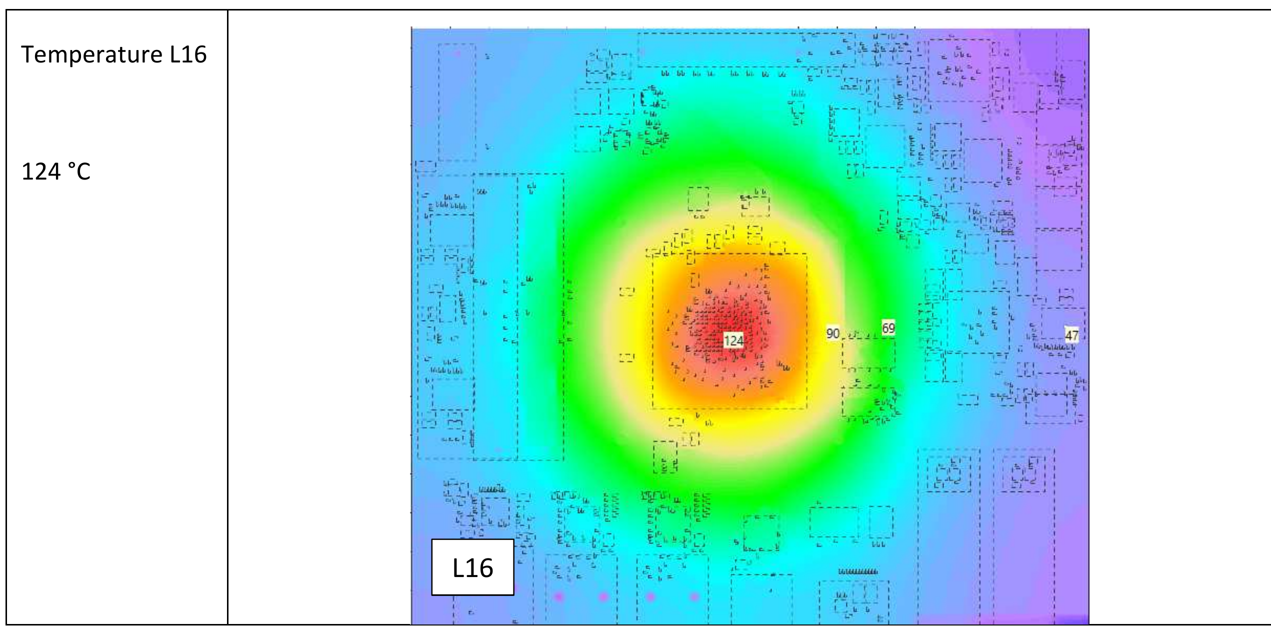
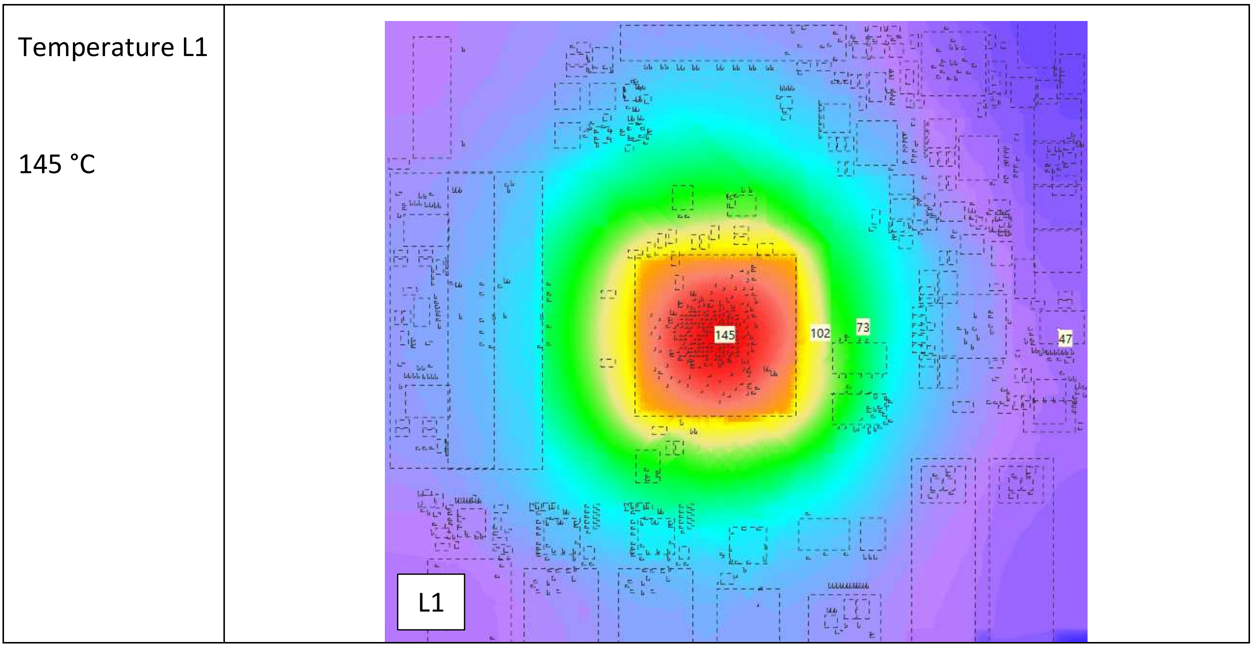


Top and bottom are about the same temperature. It indicates good thermal coupling between layers. The small boxes within the BGA contour are bottom capacitors and resistors.

Without BGA vias



In fact, it will be +20 K warmer. So the signal vias under the BGA effectively contribute to cooling.

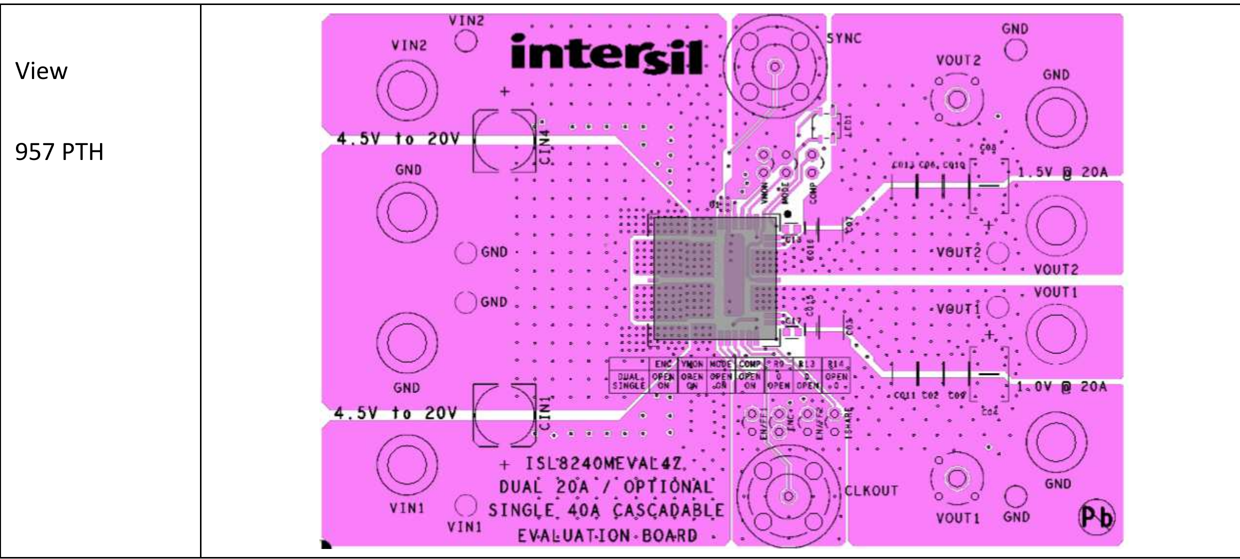
6. Intersil ISL8340

This 4-layer board has already been described as a case study (https://www.adam-research.de/dokumente/fallstudien-en/). The infrared image and the simulation agree reasonably. However, the heat spreading is hindered by the type of potential separation used, which looks approximately the same in all layers. Heat vias are therefore unlikely to be effective.

Data

View	https://www.adam-research.de/pdfs/TRM_CaseStudy1.pdf
Source	https://www.edn.com/step-down-module-delivers-100-w-from-reduced-footprint/ „The ISL8240M is a fully encapsulated step-down switching power supply from Intersil that is capable of providing up to 100 W of output power, while occupying a 17×17-mm footprint for use in infrastructure and cloud computing hardware."
Experiment 8 W 100 °C	

Model

View 957 PTH	

<table>
<tr><td>Layer stack</td><td>
<table>
<tr><th>Level</th><th>Name</th><th>Type</th><th>File</th><th>View</th><th>FR4 white?</th><th>Thick (mu)</th><th>Conductor</th><th>Dielectric</th></tr>
<tr><td>1</td><td>L1</td><td>ger</td><td>layer1.art</td><td>View</td><td>☑</td><td>70</td><td>Cu$TRM</td><td>FR4$TRM</td></tr>
<tr><td>2</td><td>pre1</td><td>pre</td><td></td><td>View</td><td>☑</td><td>210</td><td></td><td>FR4$TRM</td></tr>
<tr><td>3</td><td>L2</td><td>ger</td><td>layer2.art</td><td>View</td><td>☑</td><td>35</td><td>Cu$TRM</td><td>FR4$TRM</td></tr>
<tr><td>4</td><td>pre2</td><td>pre</td><td></td><td>View</td><td>☑</td><td>850</td><td></td><td>FR4$TRM</td></tr>
<tr><td>5</td><td>L3</td><td>ger</td><td>layer3.art</td><td>View</td><td>☑</td><td>35</td><td>Cu$TRM</td><td>FR4$TRM</td></tr>
<tr><td>6</td><td>pre3</td><td>pre</td><td></td><td>View</td><td>☑</td><td>210</td><td></td><td>FR4$TRM</td></tr>
<tr><td>7</td><td>L4</td><td>ger</td><td>layer4.art</td><td>View</td><td>☑</td><td>70</td><td>Cu$TRM</td><td>FR4$TRM</td></tr>
</table>
</td></tr>
<tr><td>Layers 1 to 4

Only compo-nent surround-ings are shown</td><td>L1 L2
L3 L4</td></tr>
<tr><td>Assumption thermal power loss</td><td>8 W , as in experimental setup
http://www.edn.com/electronics-products/electronic-product-reviews/other/4439182/Unique-Intersil-thermal-design-removes-heat-from-encapsulated--compact-50A-power-modules</td></tr>
<tr><td>Ambient</td><td>20 °C, still air + radiation</td></tr>
</table>

Calculation results

Original Viafeld

Temperature L1 104 °C The temperature color bar is similar to that in infrared imaging	
Temperature L4 94 °C	

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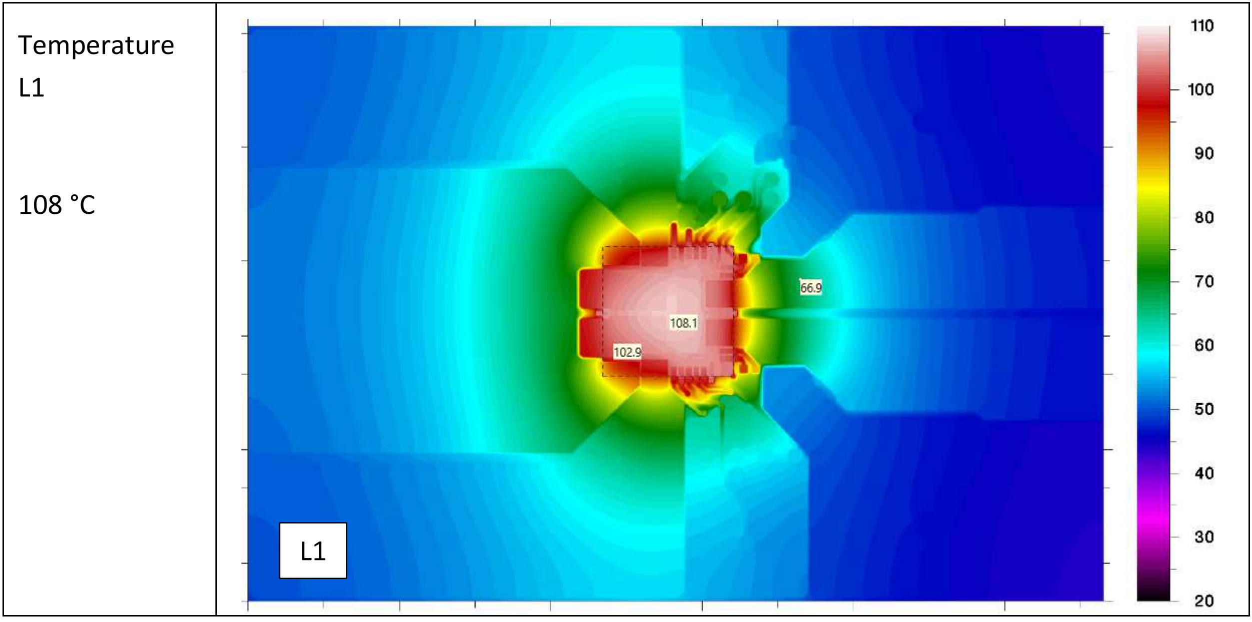
Without any via



In fact, without any vias, it gets +4 K warmer only. So almost no via contribution to cooling here.

References

There are many sources and documents on the Internet about the topic of heat vias. Here just a brief selection.

[1] "A Quick PCB Thermal Calculation for Power Electronic Devices with Exposed Pad Packages" (2017) https://www.onsemi.com/pub/Collateral/AND9596-D.PDF

[2] Ellison, G.N.: *Thermal computations for electronics*. Boca Raton: CRC Press, 2011

[3] Stout, R.: "Thermal Considerations for a 4x4 mm QFN" (2009) https://www.onsemi.com/pub/Collateral/AND8432-D.PDF

[4] TRM Thermal Risk Management. https://www.adam-research.de/en/software/

[5] "Understanding Thermal Analysis of RF Devices" (2023) https://www.qorvo.com/resources/d/understanding-thermal-analysis-of-rf-devices-application-note (with links to video and web calculator)

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